Different concept of D/A-conversion and circuit aspects of a specific 20b DAC

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Outline

- Basics of Data Conversion (ADC, DAC)
- Specification Parameters of DACs
- Simplest DAC architectures
- Design Challenges of high-speed and high-accuracy DAC
- Oversampling DAC for high precision applications
- Example of a DAC System and Circuit Design
- Summary

Basics of Data Conversion

Each digital signal processing system needs
a data acquisition channel: ADC and/or DAC

The circuit design of ADC and DAC is the
most challenging field in analog integrated systems:

- each additional bit of accuracy corresponds to
  a doubled precision requirements

  10bit = 2^{-10} = 0,1%

  20bit = 2^{-20} =1ppm
- design of data converters needs deep understanding
  of their spectral properties (system theory)

Basics of Data Conversion

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a data acquisition channel: ADC and/or DAC

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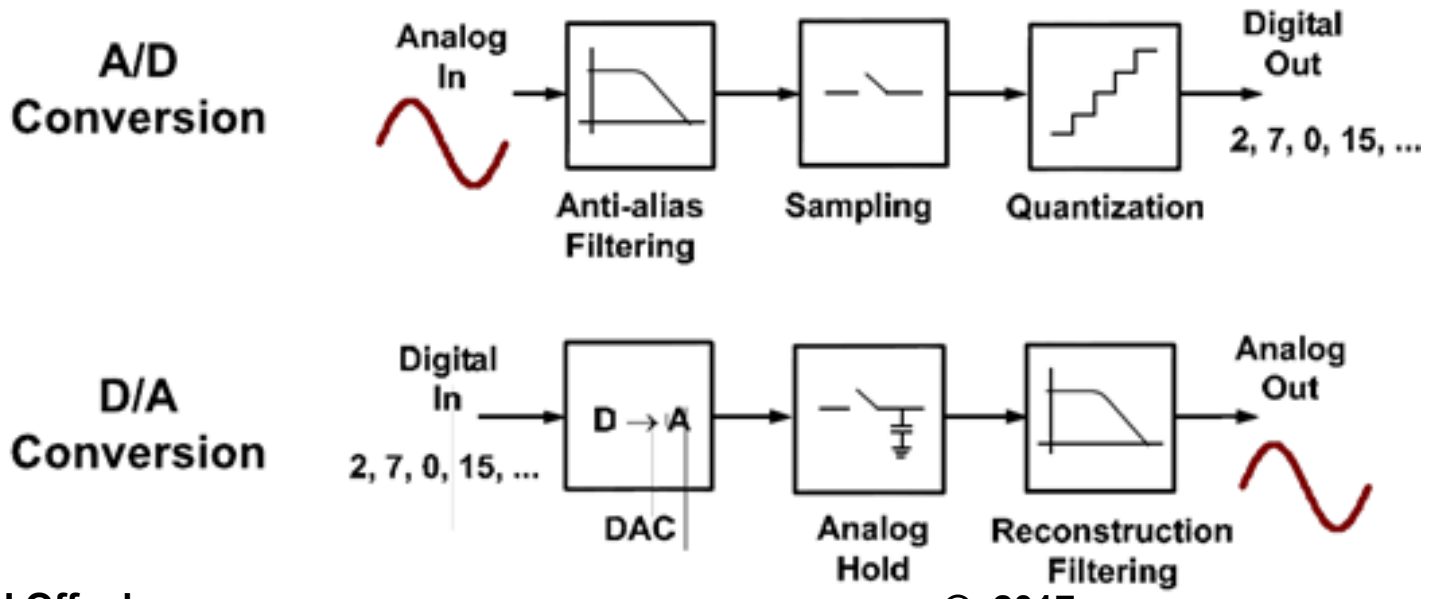
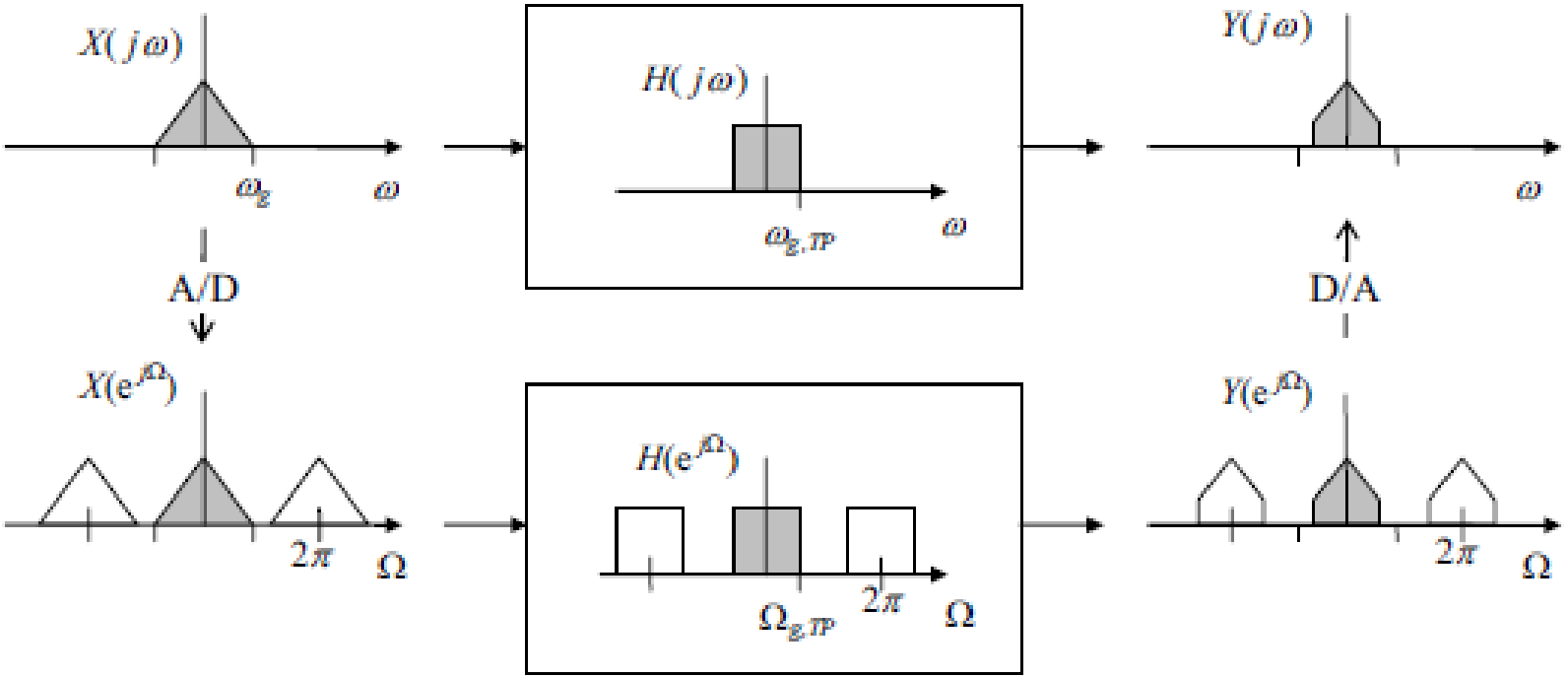


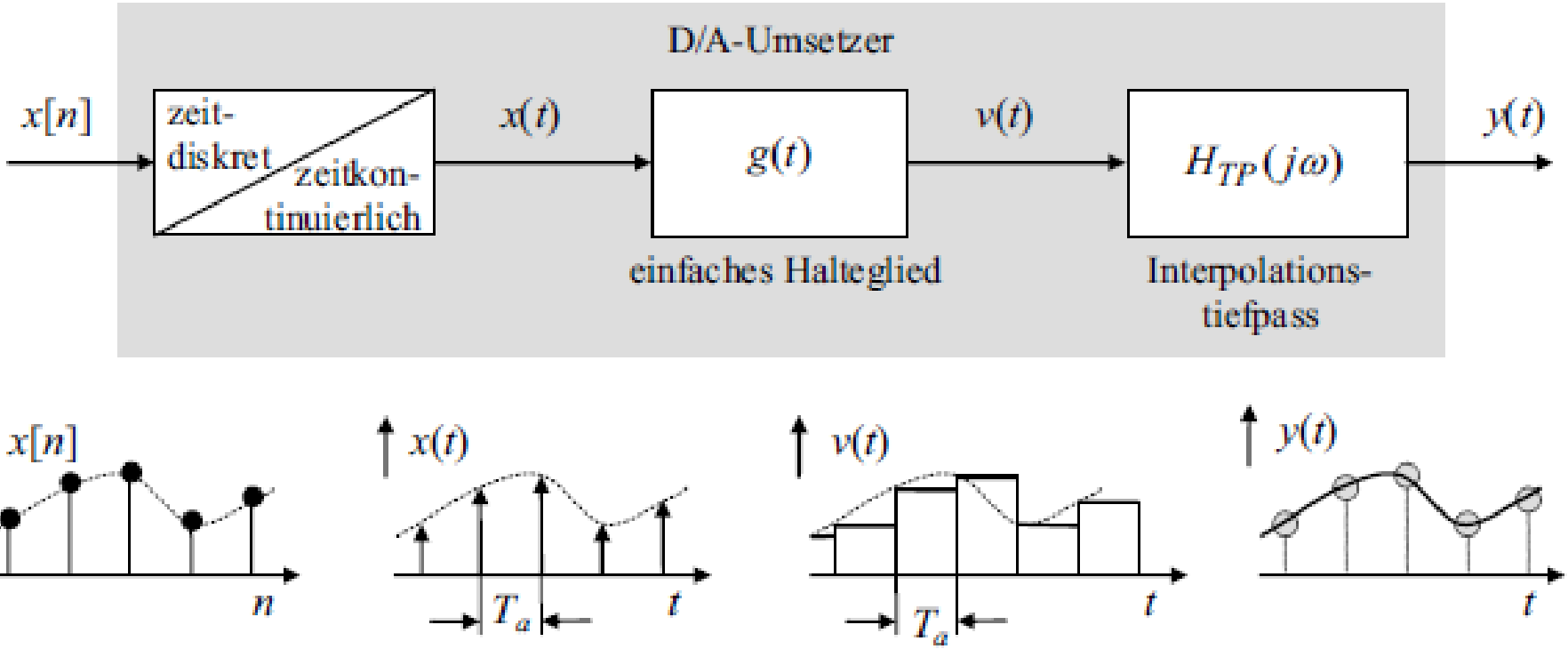
Basics of Data Conversion

Spectral properties of ADC / DAC signal processing system



Basics of Data Conversion

Signal processing steps of a DAC

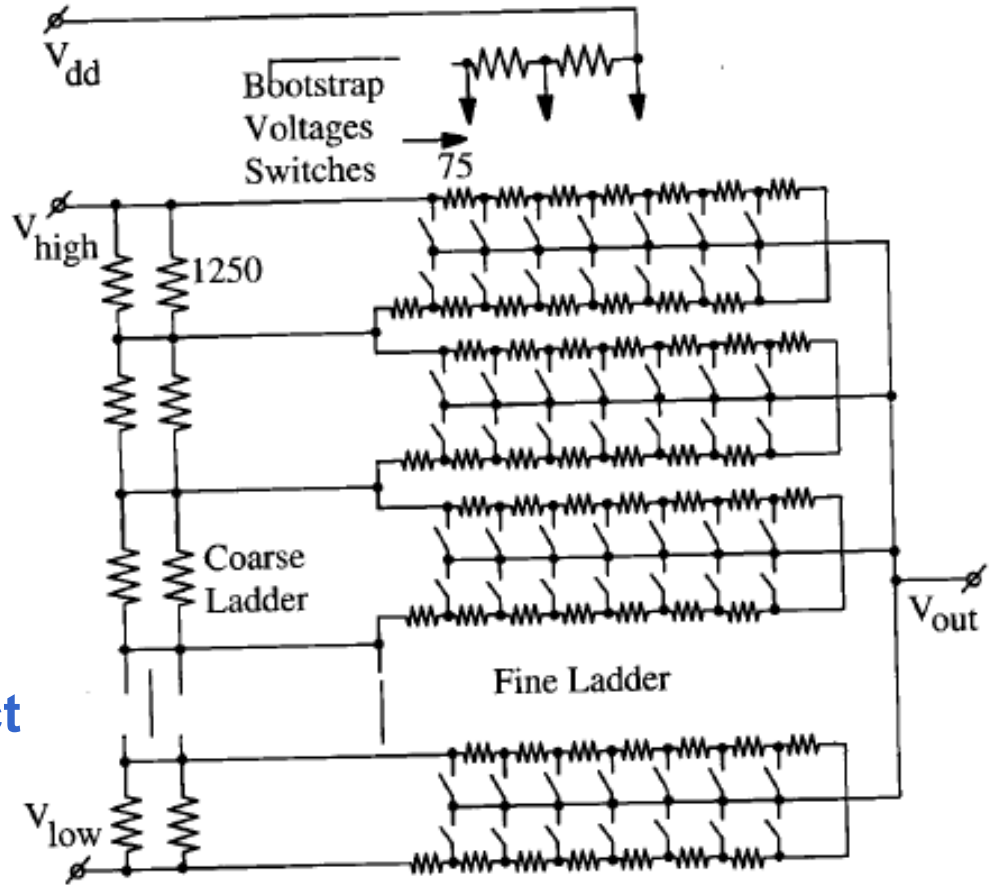


Basics of Data Conversion

Example of a simplest DAC: Resistive ladder network

10bit DAC:
•coarse ladder with 16 accurate taps (dominating the linearity)
*** matrix of 32x32 fine ladder resistors, each 64th tap connected to coarse ladder**

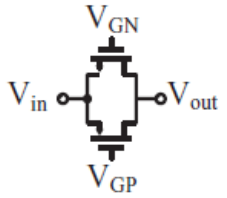
only few countermeasures to compensate the mismatch effect causing nonlinearity (INL)

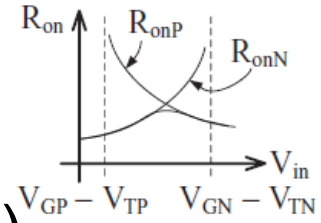


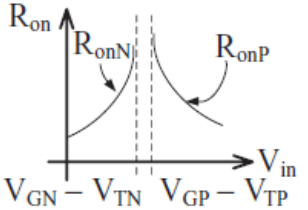
CMOS Scaling challenges

Modern submicron CMOS technologies causes problems with:

- decreased Gox thickness => decreased Vdd
- decreased Vdd => decreased signal range
- decreased Vdd => switch resistance increases
- degraded intrinsic gain gm/gds
- velocity saturation (no unlimited current pushing)
- increased gate current leakage (due lowering Vth)
- DIBL => degrades the D-side output impedance







- increased unity gain frequency
- Improved matching for MOS transistors and MiM caps

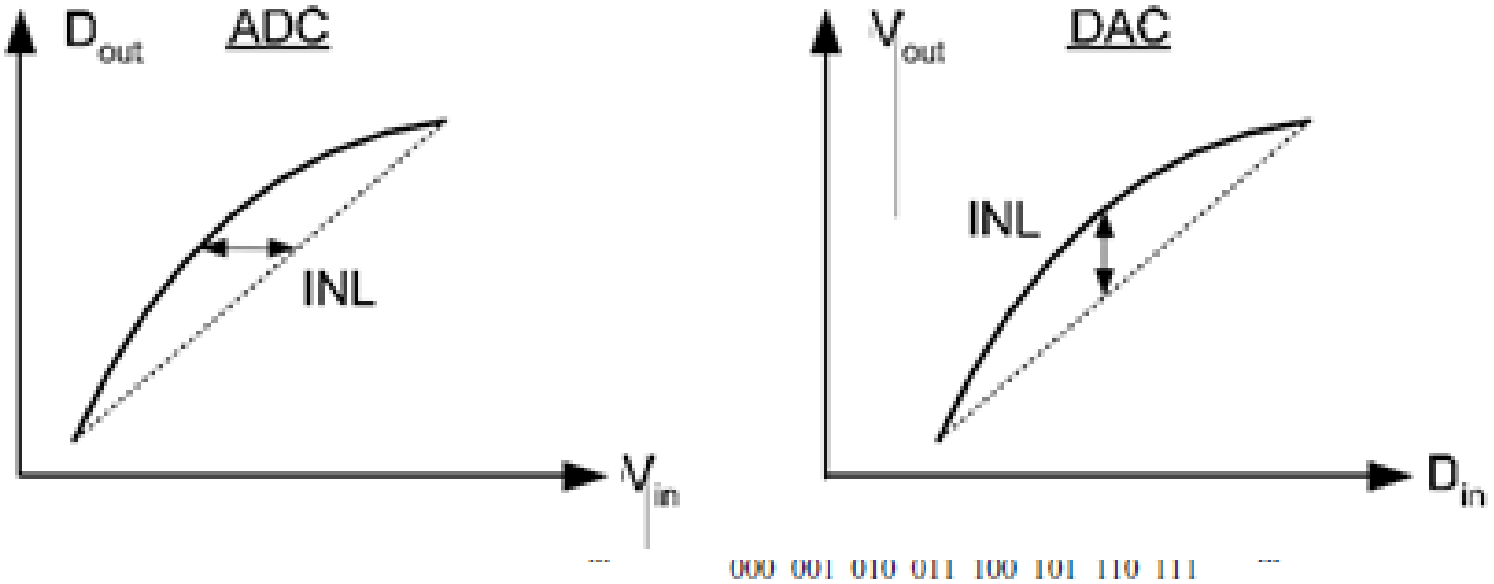
=> demand for new data conversion architectures

DAC specification parameters

DAC static parameters: linearity of conversion curve

Deviations from linear mapping of Din to Vout (straight line)

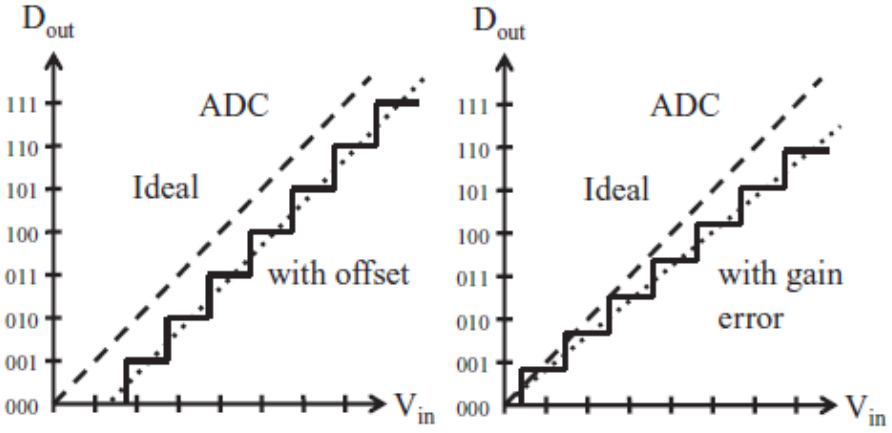
Similar to ADC parameter definition => only all DAC errors are estimated as vertical y-axis deviation



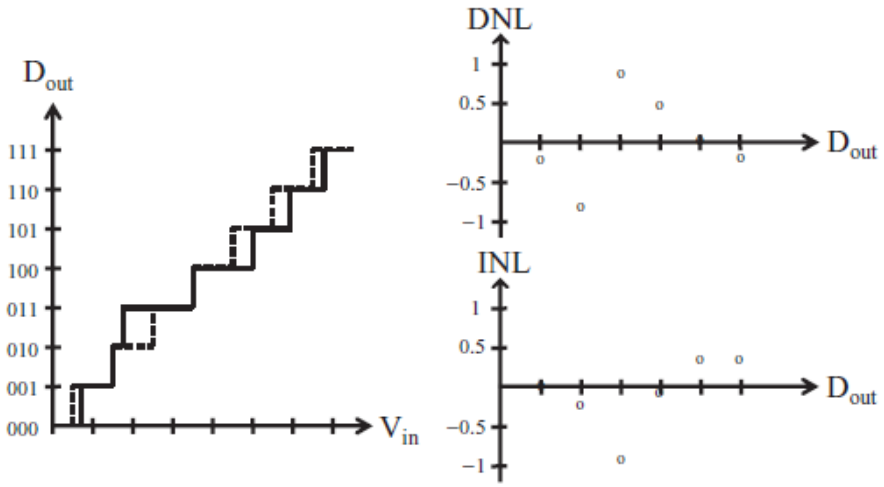
DAC specification parameters

Static parameters

- DAC offset error (zero shift), DAC gain error (curve slope)



- Integral (INL) and Differential (DNL) Non-Linearity



D/A converter:

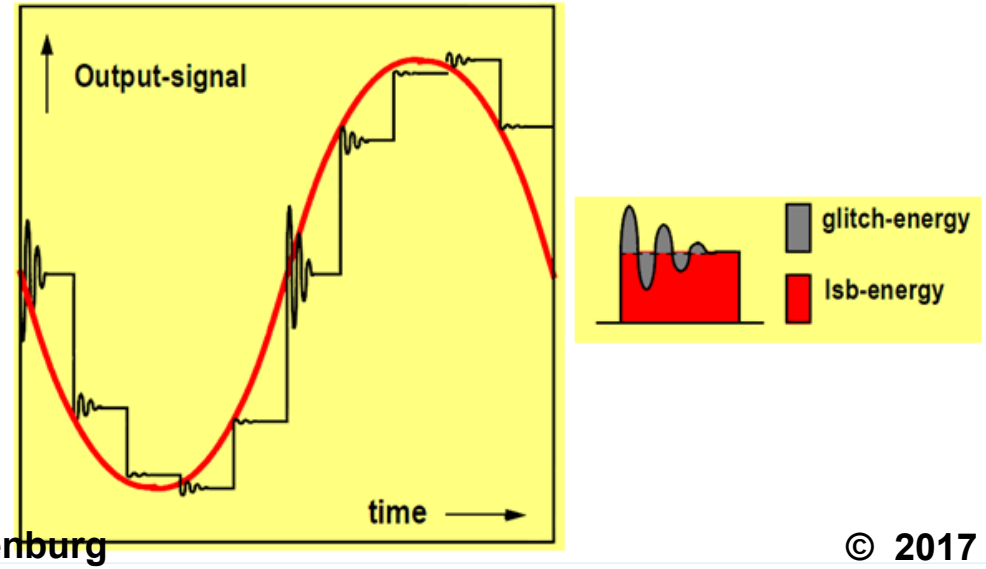
- DNL < -1LSB implies non-monotinicity
- If all codes |INL| <0.5LSB => all |DNL|<1LSB

DAC specification parameters

Dynamic Performance Metrics

- Time domain: glitch impulse, aperture uncertainity, settling time
- Frequency domain: SNR, THD, IM2/IM3, SFDR, SNDR (ENOB)

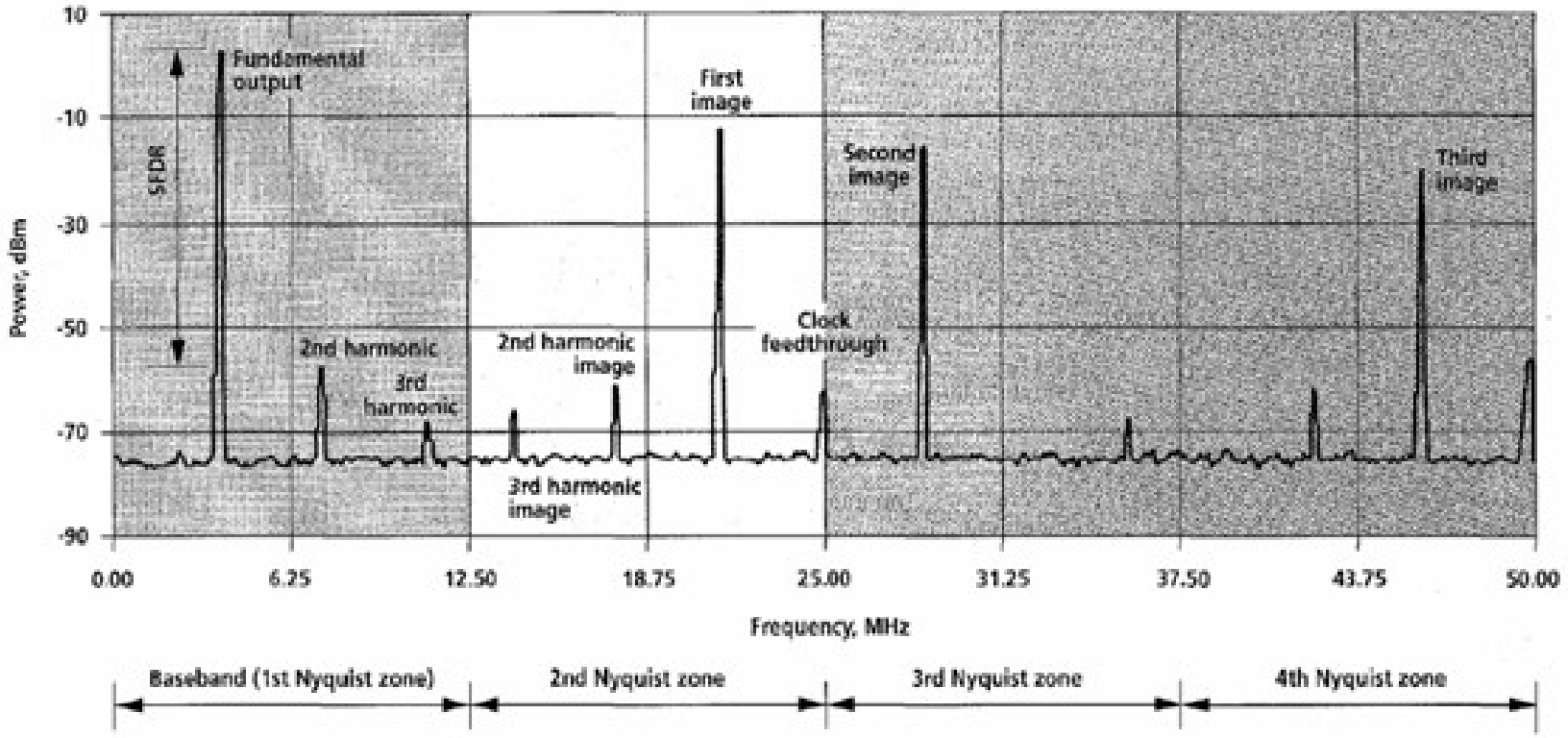
- Important to realize: both static DNL & INL and dynamic errors contribute to frequency domain non-ideality



DAC specification parameters

Dynamic Performance Metrics

- Frequency domain: SNR, THD, IM2/IM3, SFDR, SNDR
- noise, distortion, spurs, noise & distort.



[Hendriks, "Specifying Communications DACs, IEEE Spectrum, July 1997]

DAC specification parameters

Dynamic Performance Metrics

- Frequency domain:

  $SNR = 20 * \log (P_{sig}/P_{noise})$ in + dB values

  $THD = 20 * \log (P_{harm}/P_{sig})$ in – dB values

  $SNDR = 20 * \log (P_{sig}/P_{harm}+P_{noise})$ in +dB values

  $SFDR = 20 * \log (P_{sig}/P_{dist\_max})$ in +dB values

  SNDR [dB] = 6,02 * ENOB + 1,76dB

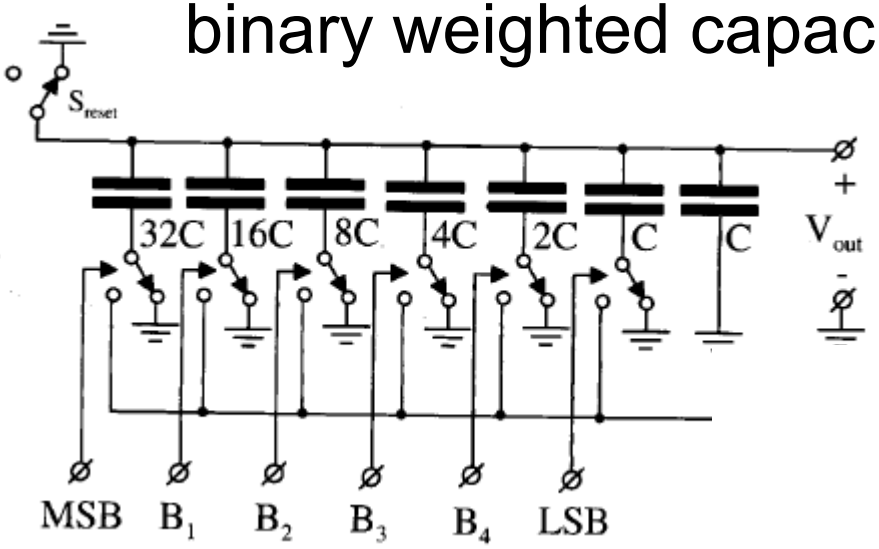
Recalculation of Signal purity (SNDR) to effectite number of bits

const. therm. noise density => with increasing DAC bandwidth SNR deteriorates (limit the bandwidth as low as needed)

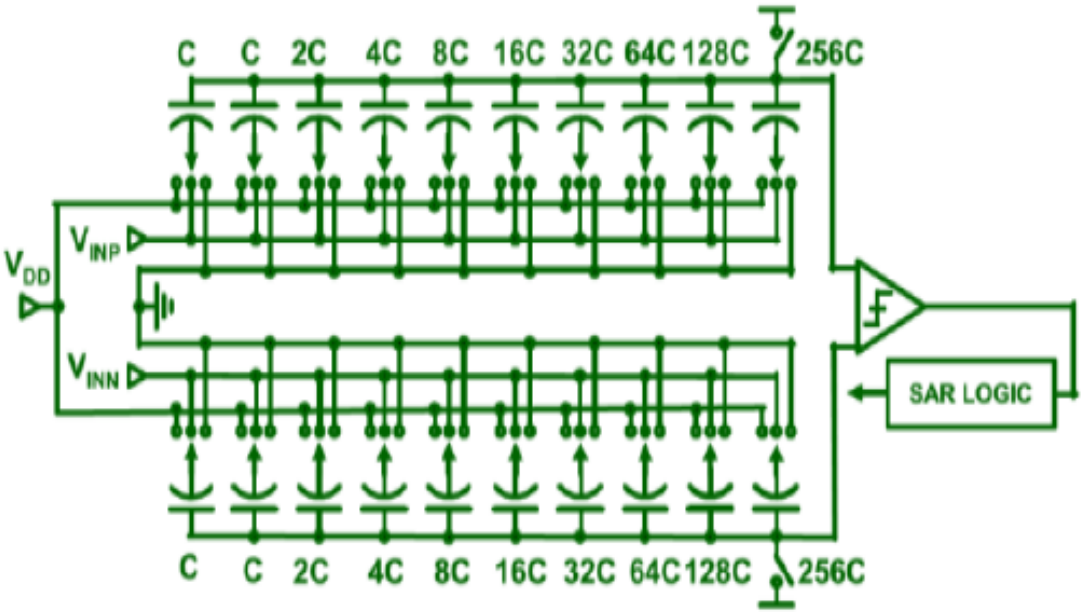
$ND\ [dBFS/Hz] = – SNR – 10.\log (f_s/2)$

DAC architectures

Capacitive DAC: used within the SAR ADC in FB-loop; binary weighted capacitors require large area

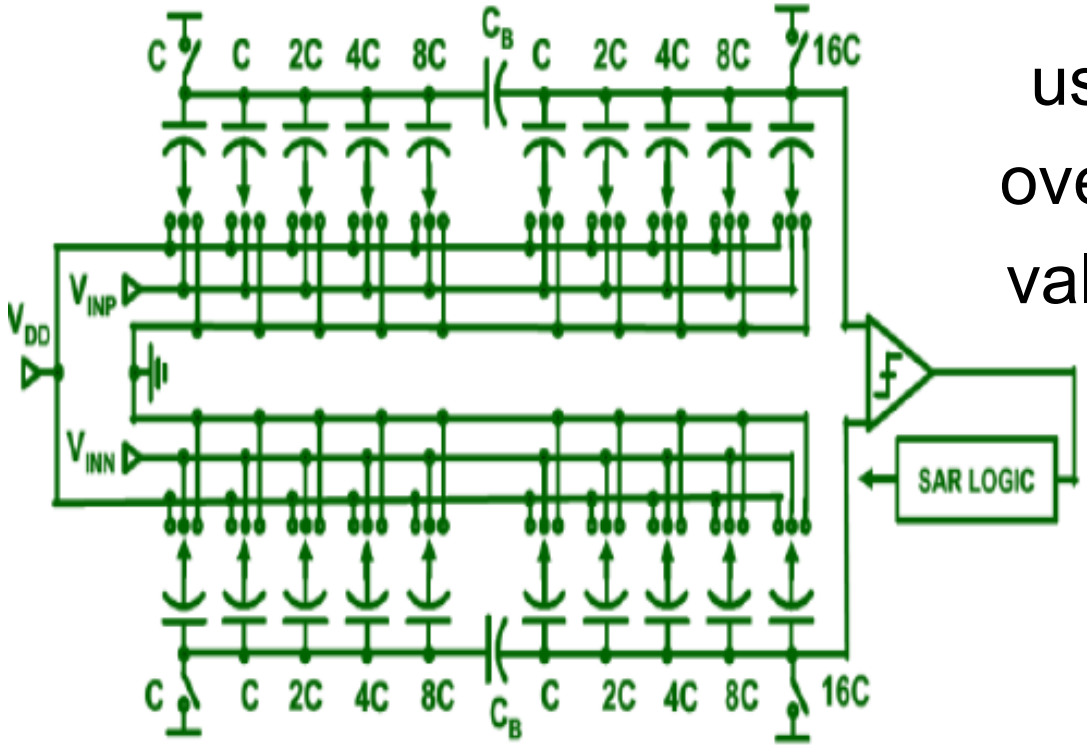


DAC cap-array is re-used as the sampling capacitor @ ADC input (hard to drive 30-50pF)



DAC architectures

Bridged Capacitive DAC of a SAR ADC



used to decrease overall capacitance value in DAC array

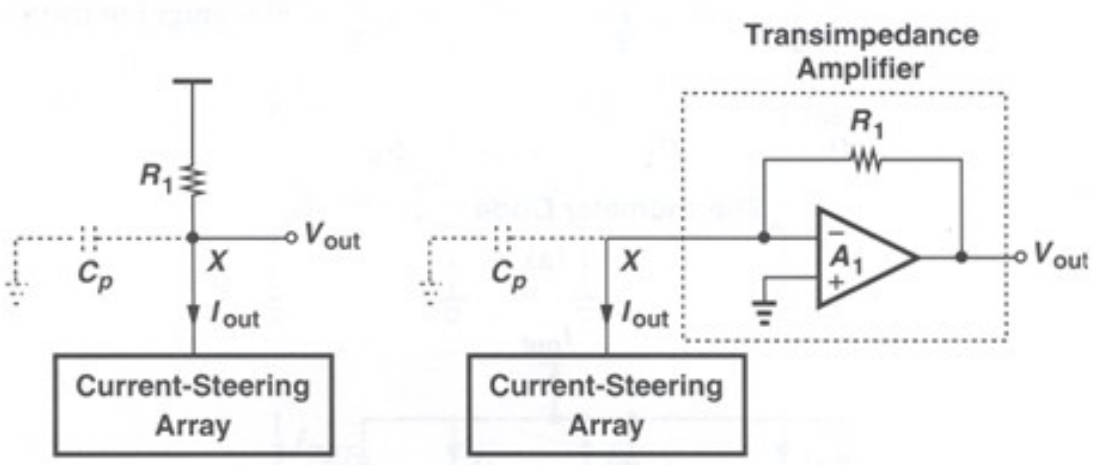
Further SAR-ADC modification:

Non-binary cap-DAC, Dual-trial cap-DAC, Split-cap-DAC

Current Steering DACs

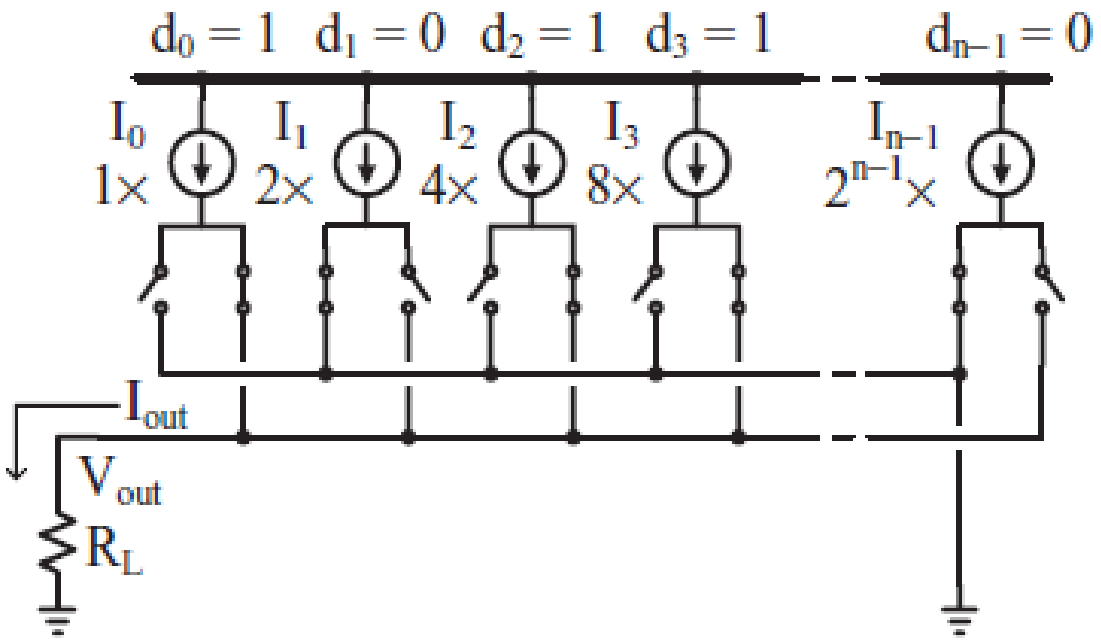
Recently most used architectures: for high-speed and/or high-resolution DAC

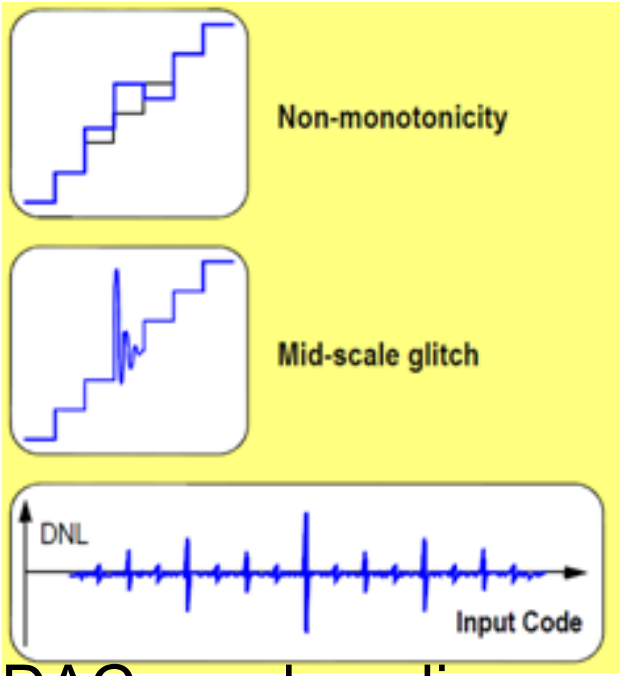
- inherent high speed operation of MOS current sources
- ability to drive low-impedance nodes
- benefits from improved matching in submicron CMOS
- active cells able to compensate in easier way



Current Steering DACs

Binary weighted current cells:





+ Simple architecture: N cells for N-bit DAC; no decoding logic required

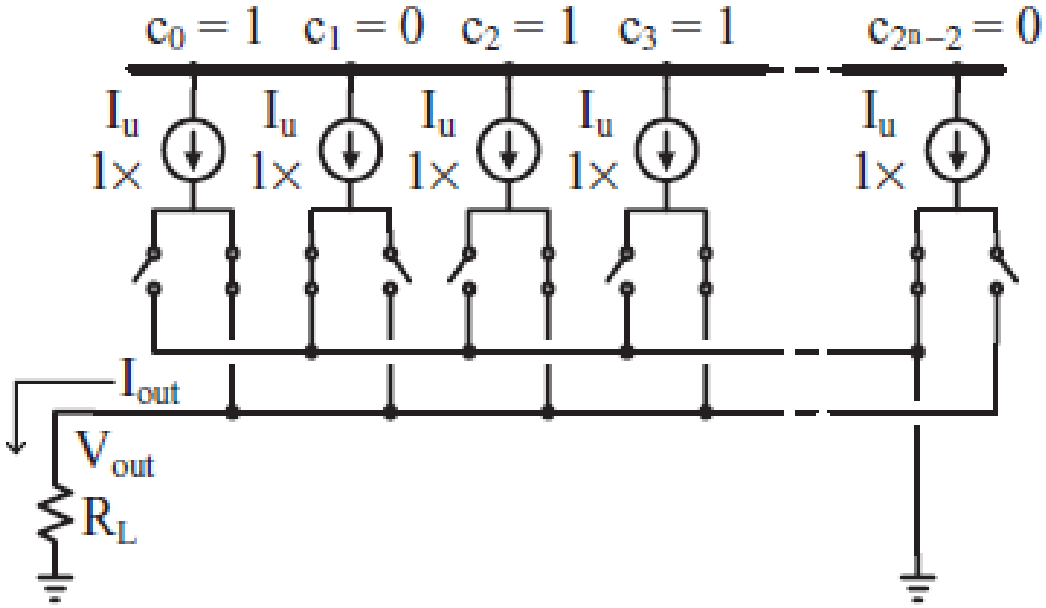
- Code transitions cause glitches

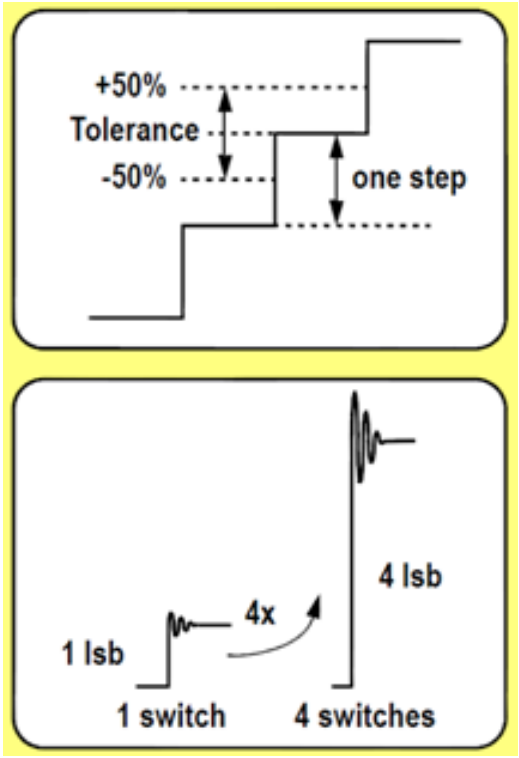
- Non-matched current cells causes non-linearity

(=> large cell area to achieve a certain linearity)

Current Steering DACs

Thermometer decoded current cells:

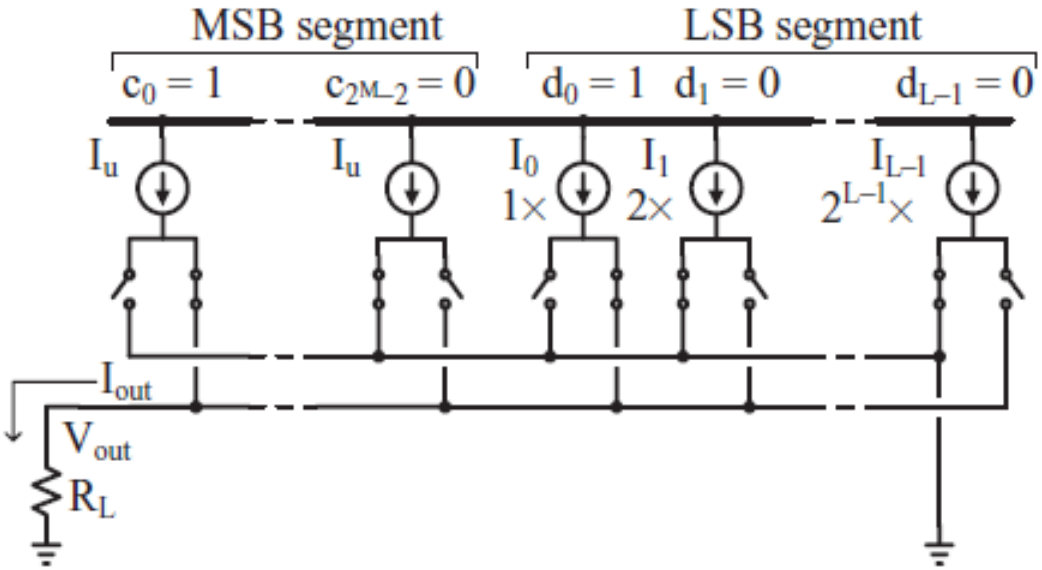




+ Guaranteed Monotonic, INL same as binary
+ at major code transitions (MSB) only 1 current cell switched
+ Matching: 50% good enough for DNL<1/2 LSB
- Increased area due to large amount of cells: 10bit = 1024 cells
- Decoding logic required (power & area compromise)

Current Steering DACs

Segmented current cells:



3-6 MSBits encoded into thermometer code using equal current cells => improves the monotonicity of DAC

- Increased monotonicity on the expense of increased nr. of elements: 3bit binary vs. 8 elements thermometer / 5bits binary vs. 32 equal elements

+ relaxed current cells area due to relaxed matching requirements

Current Steering DACs

Segmented current cells:

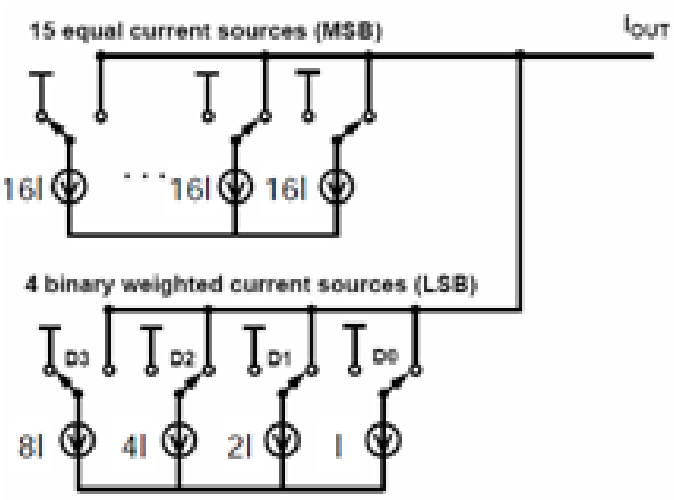
INL same as in thermometer DAC

DNL:

*Worst case occurs when LSB-cells turns off and one more MSB cell turns on

*Essentially same DNL as binary weighted DAC with B_{bin}+1 bits

Example: $B=B_b+B_l=4+4=8$



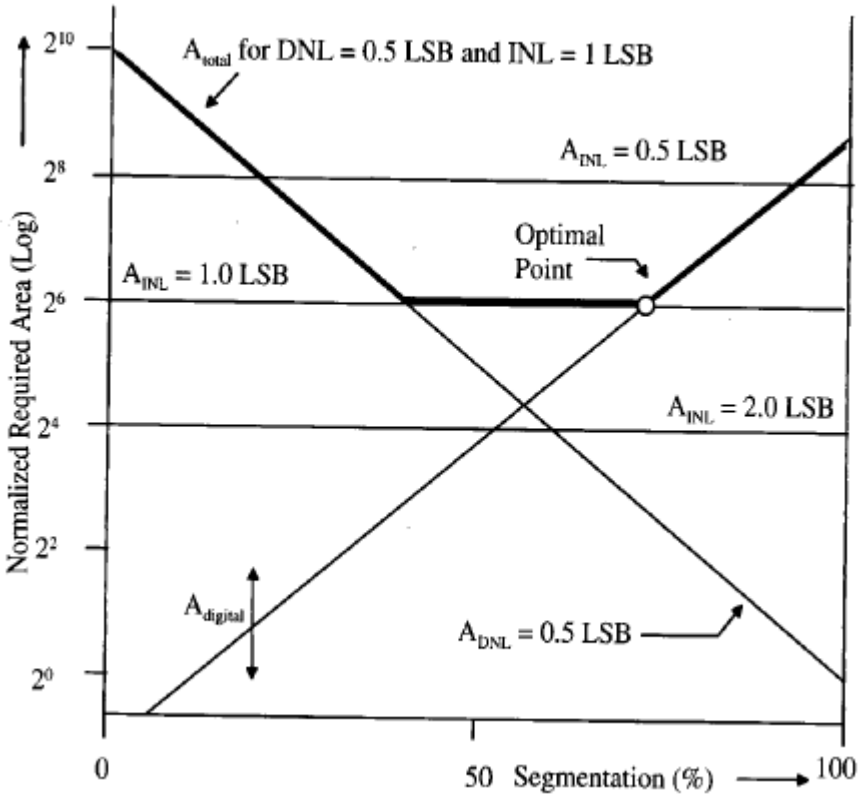
Current Steering DACs

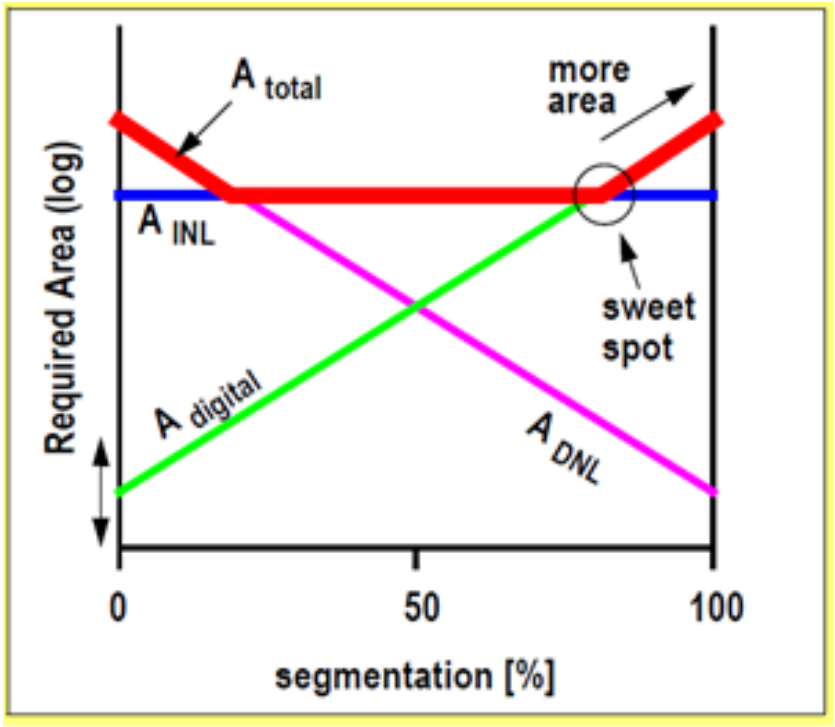
Segmented current cells: Design Trade-Off

	Thermometer	Segmented	Binary Weighted
σ_{INL}	$\cong \frac{1}{2}\sigma_u\sqrt{2^B}$		
σ_{DNL}	$\cong \sigma_u$	$\cong \sigma_u\sqrt{2^{B_b+1}-1}$	$\cong \sigma_u\sqrt{2^B-1}$
Number of Switched Elements	2^B-1	$B_b+2^{B_t}-1$	B

Current Steering DACs

Segmented current cells: Design Trade-Off





<u>Segmenation impacts:</u>

Area (cell size and number of cells)

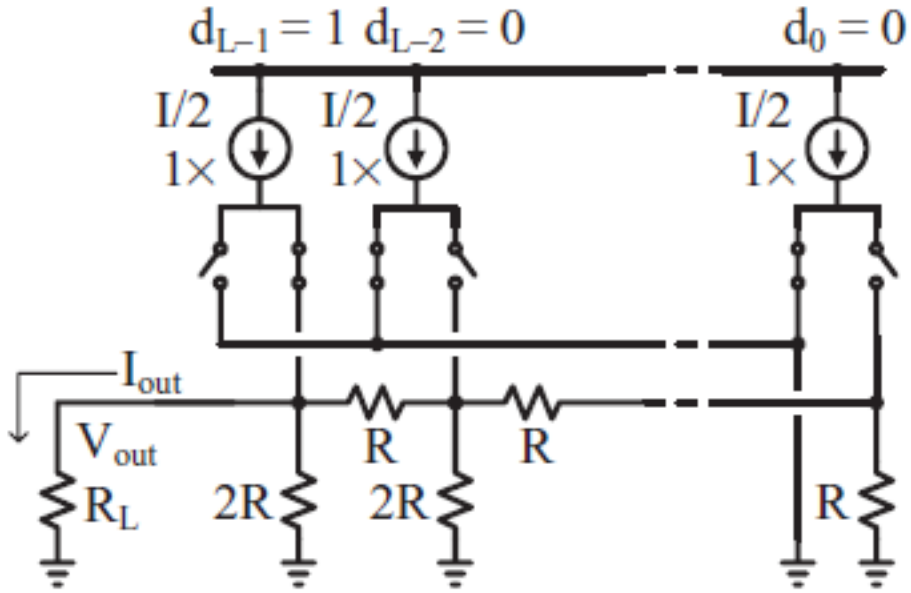
Power consumption

Distortion performance

Current Steering DACs

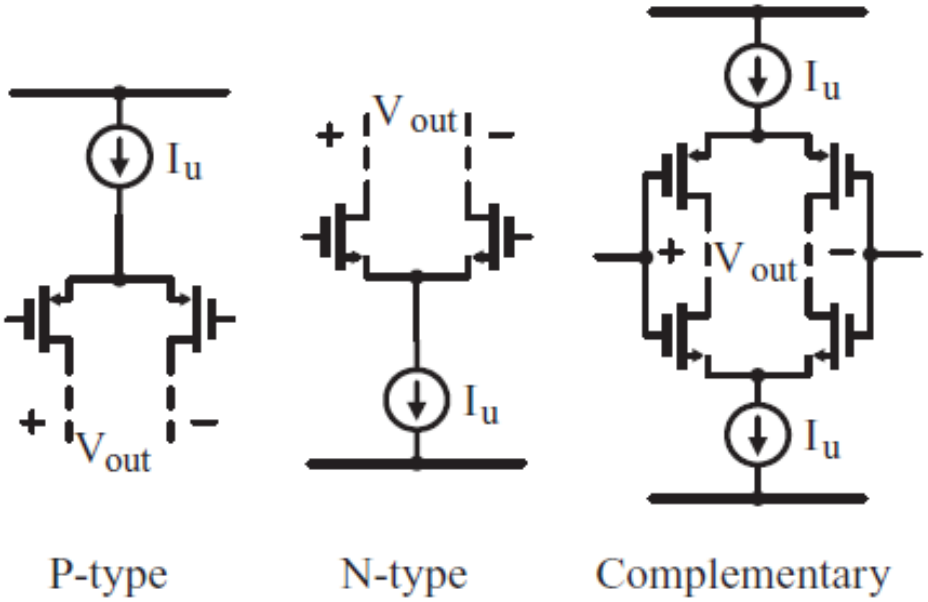
Binary weighted DAC with unitary currents

but R-2R loading network



Current Steering DAC Cell

Current Steering DAC cell architecture



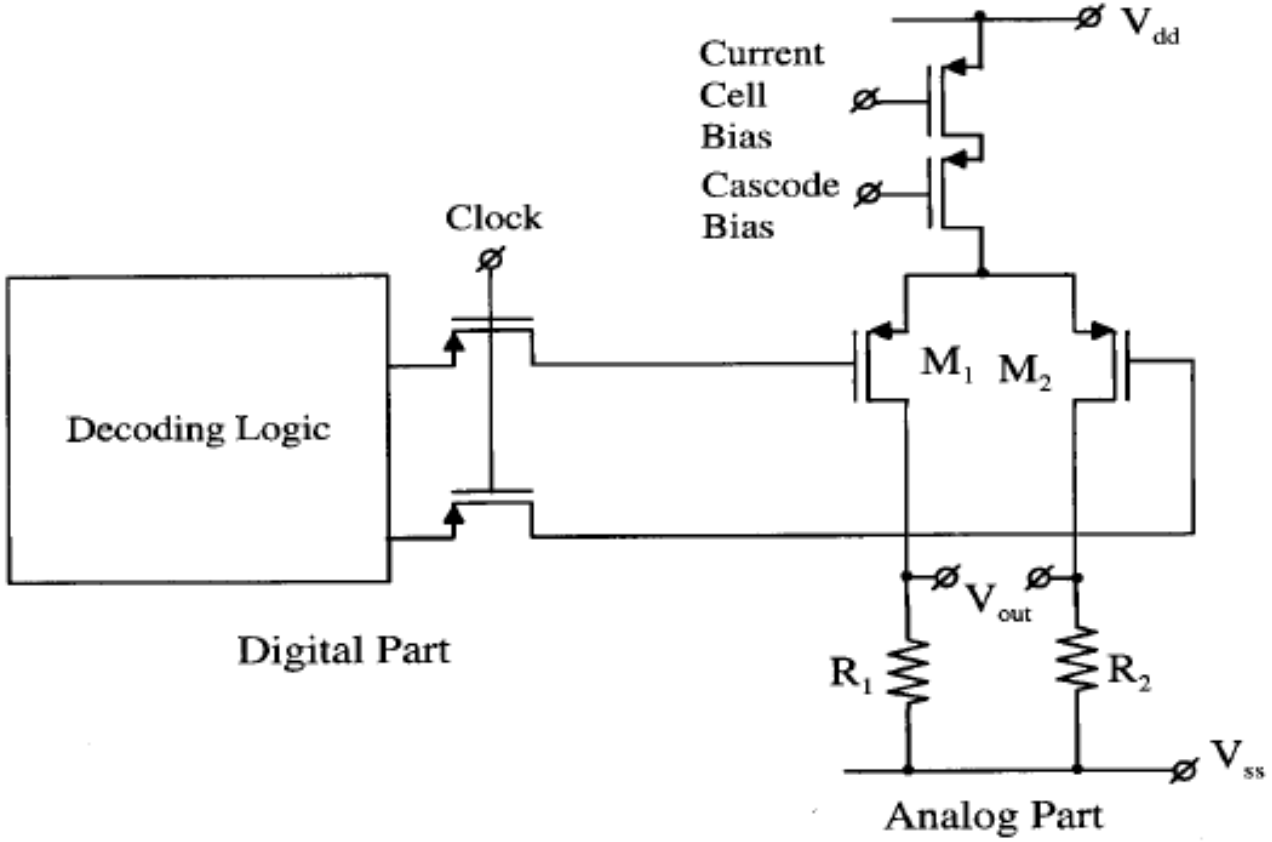
P-type N-type Complementary

Depending on the required accuracy different topologies are used:

- Current source cascoded
- Switched operated in triode or in saturation (++)
- Unipolar or bipolar current flows
- RZ or NRZ switching

Current Steering DAC Cell

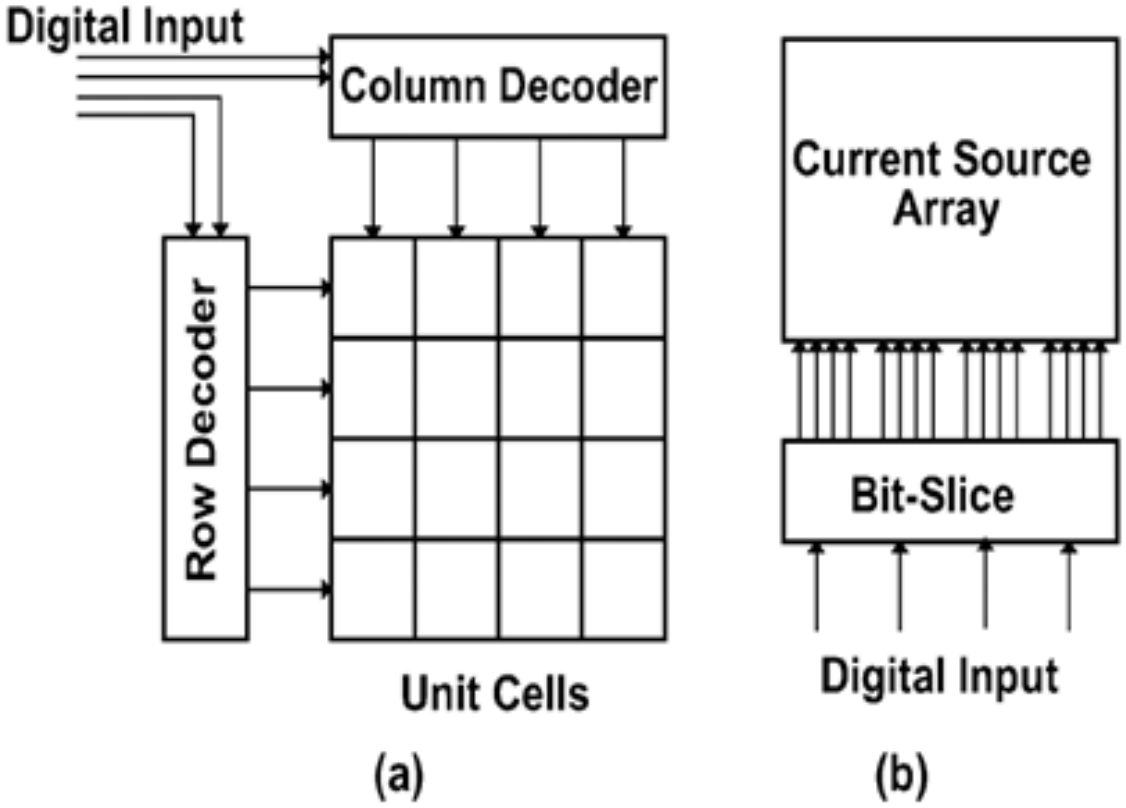
Current Steering DAC cell architecture



Matching: ΔVth and geometric matching (ß=u.C_{ox}.W/L)
ΔVth dominant => large gate overdrive voltage operation

Current Steering DACs

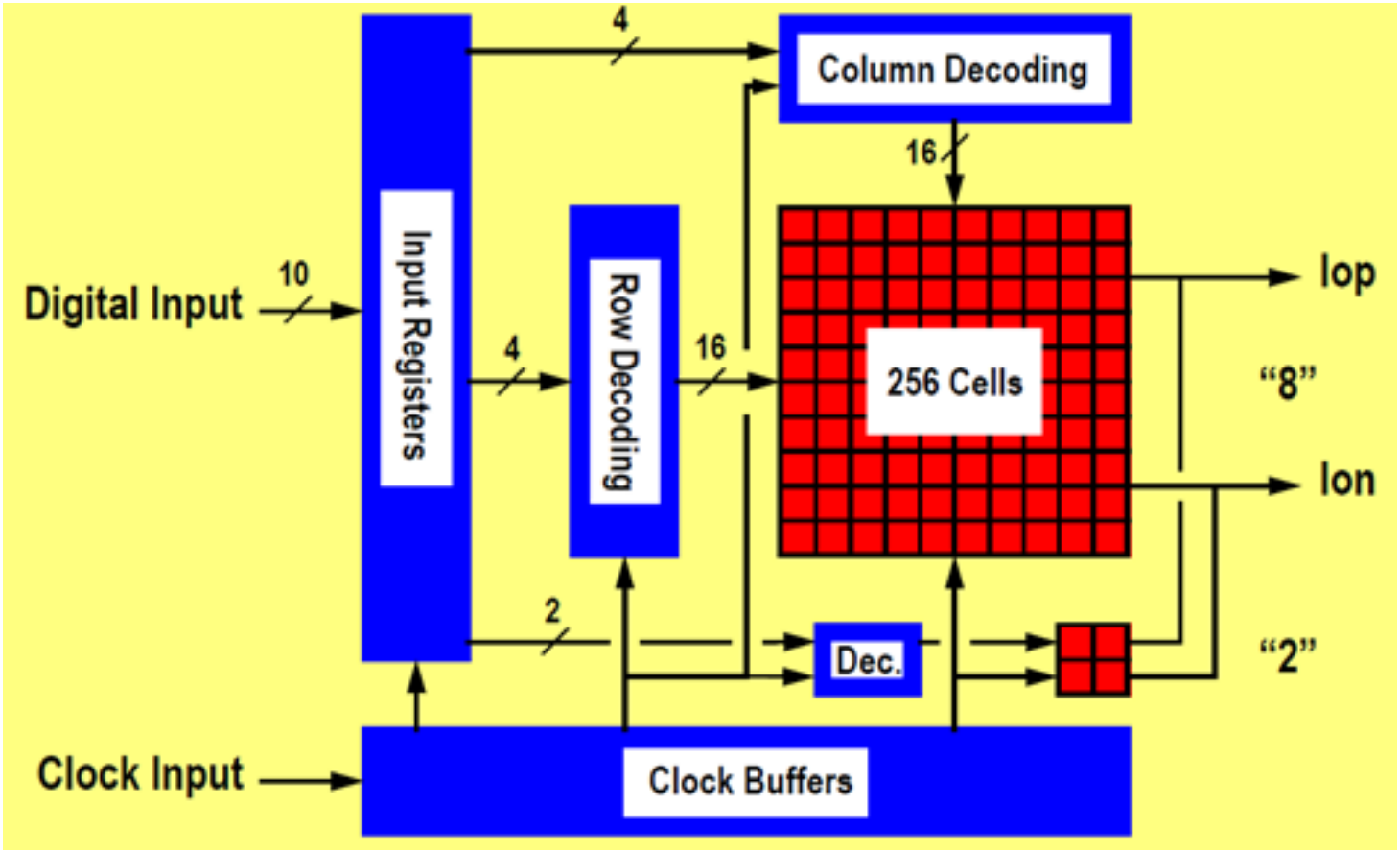
Some ideas on floorplaning in the layout



a) Row and column floorplaning (switch & cell together)
b) Current source array separated from switches

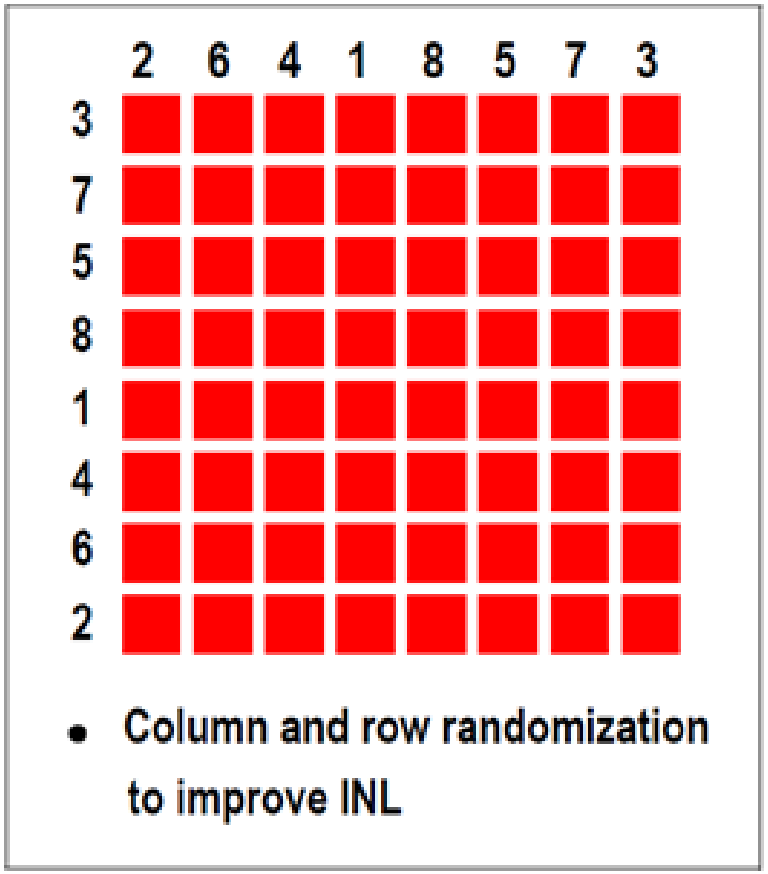
Current Steering DACs

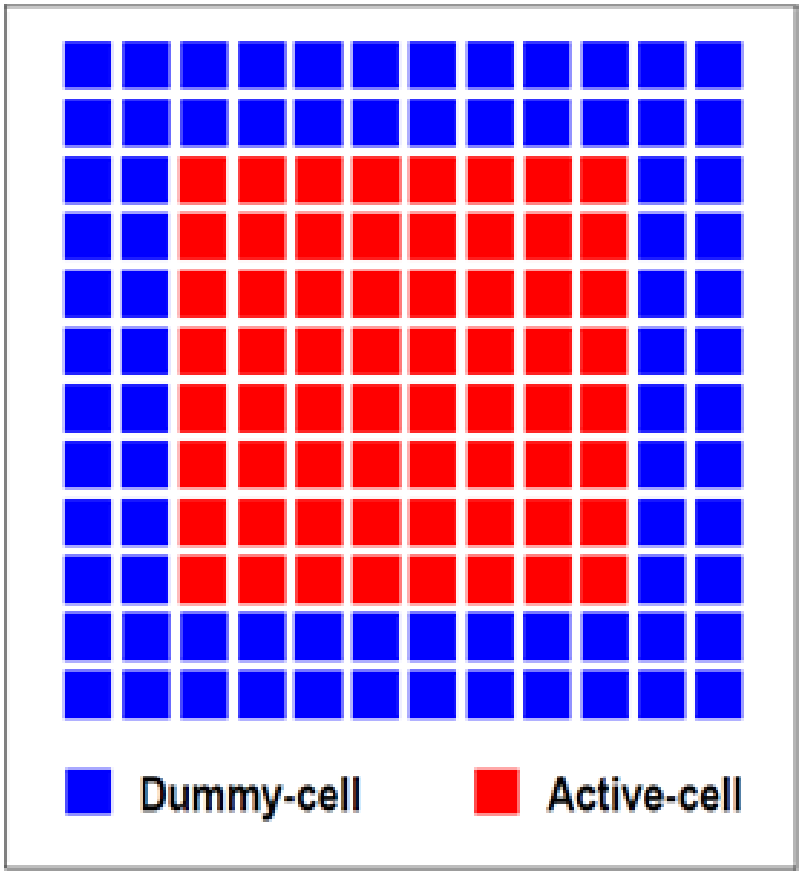
Some ideas on floorplaning



Current Steering DACs

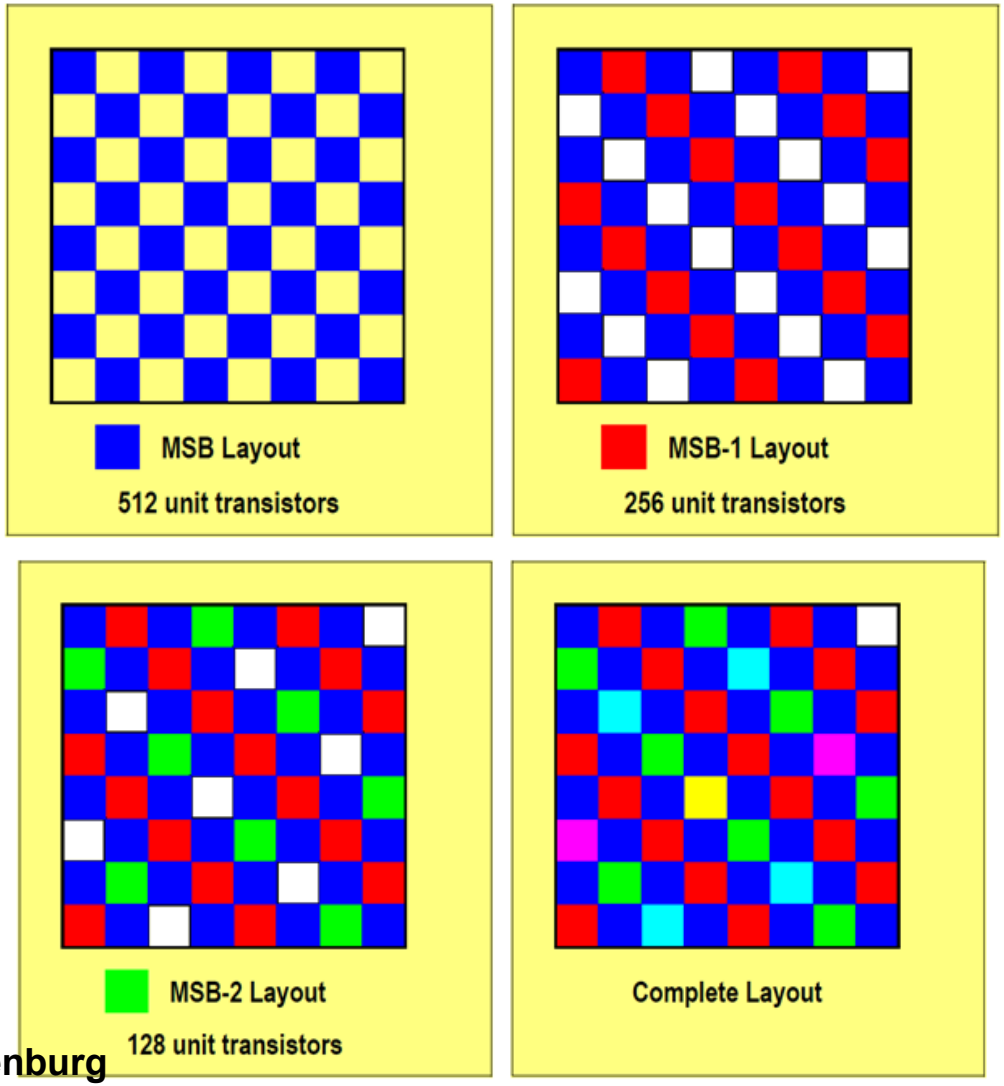
Cell Layout floorplaning





Current Steering DACs

Cell Layout floorplaning



Current Steering DACs

Error source of the current pulse at output

Amplitude Errors:

- Transistor mismatch (cell-to-cell)
- IR-drop on supplies (resistor in Vdd-path to cells)
- Finite output impedance of the cell
- Supply Disturbance (switching noise)
- Device Noise

Timing errors:

- Switch driver mismatch (edge steepness)
- Clock jitter
- Device Noise, Supply Noise

DAC specification parameters

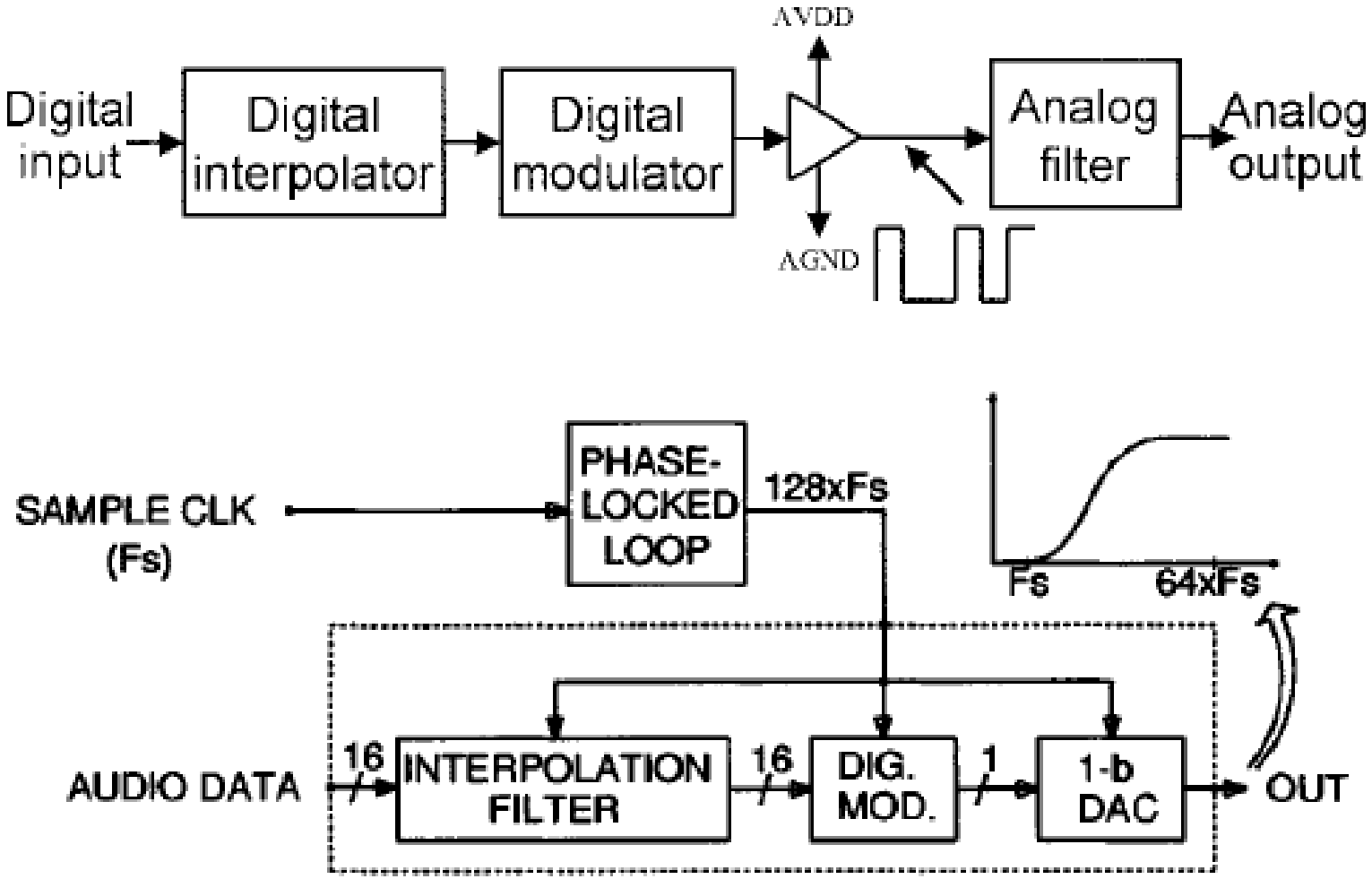
Parameter	Typical value [unit]
DAC & Postfilter-Buffer Resolution	20 bit, effect. used 19.6 bit
DAC & Postfilter-Buffer Accuracy	16 bit
SNR (signal to noise ratio) in 300kHz band	96 dB @ -1dB FS 1kHz sin
DAC output voltage noise after Filter & Buffer	400µV_{pp} @ 20MHz BW
THD (Total Harmonic Distortion)	-100dBc @ -1dB FS 1kHz sin -90dBc @ -1dB FS 10kHz sin -80dBc @ -1dB FS 100kHz sin -70dBc @ -1dB FS 1MHz sin
Spurious Free Dynamic Range (SFDR)	-120 dB over 20MHz
DAC &Buffer DNL (differential non-linearity) @ 20Bit	< 1 LSB (monotonic @ 20 bit level)
DAC &Buffer INL (differential non-linearity) @ 20Bit	< 32 LSB (monotonic @ 20 bit level)
DAC glitch energy	nom. 200 pVs / max. 500 pVs
DAC Sampling rate fs	100 MS/s
DAC Data input rate	variable 5-10-20 MS/s

Current Steering ΣΔ-DACs

To achieve the 20b linearity requirements as well as the SNR of 96dB in 300kHz, a complete different approach has to be used, when the power consumption and required chip area should not overwhelm the design.

Using Sigma-Delta Modulation digital data stream is oversampled and applying this high-speed data stream to a single bit DAC-cell with subsequent filtering allows to achieve superior linearity.

Current Steering ΣΔ-DACs



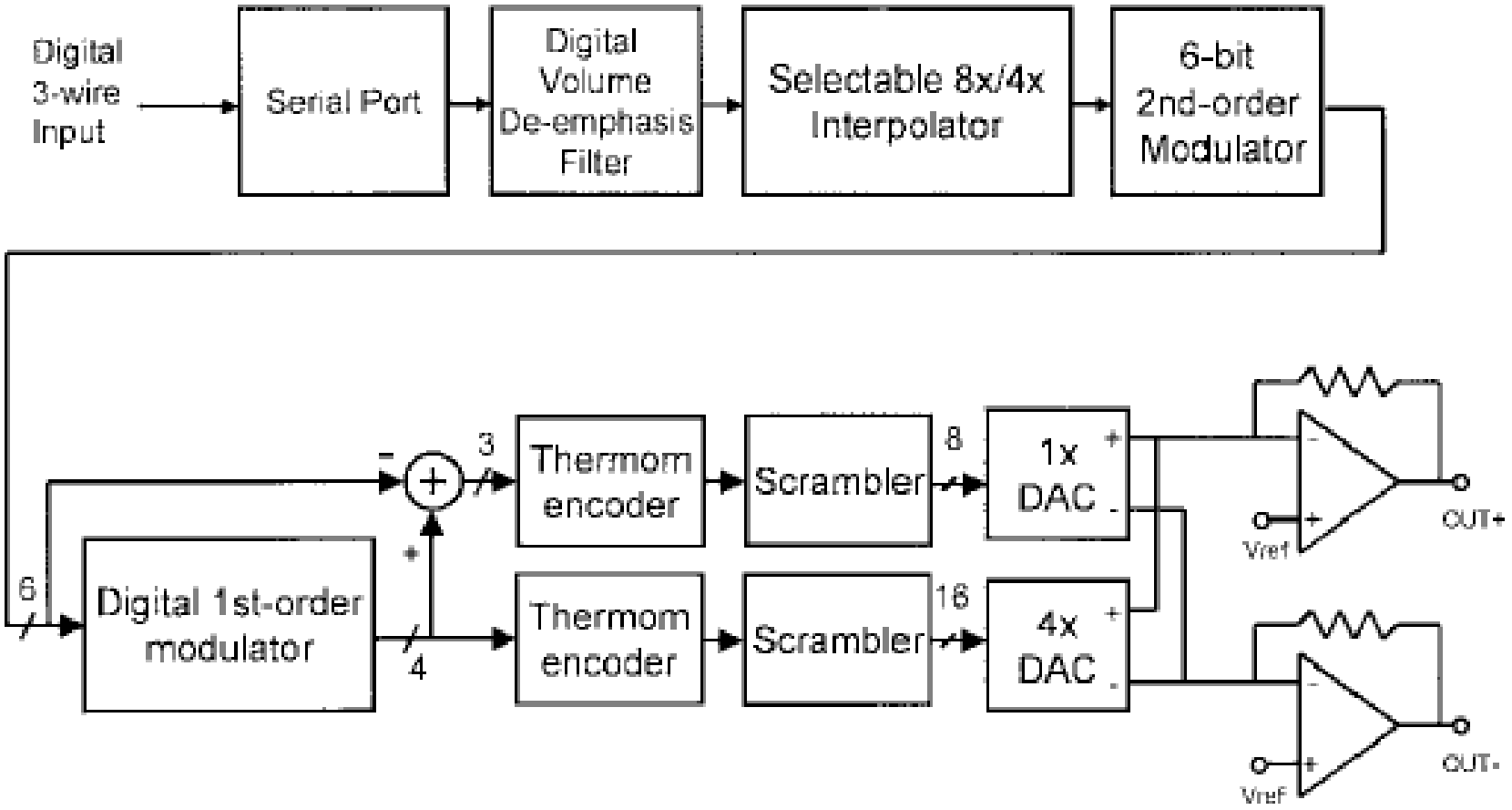
Current Steering ΣΔ-DACs

+ in-band noise shaped => decreased
+ inherent linearity with single-bit DAC cell
+ decreased number of cells, even with ΣΔ-Modulator
  with 5 bit output (32 current cells)

- Increased out-of-band noise (analog filtering needed)
- Increased frequency of operation (jitter)
- A high speed data stream has to be provided (interpolation)
- Increased power consumption due to high speed

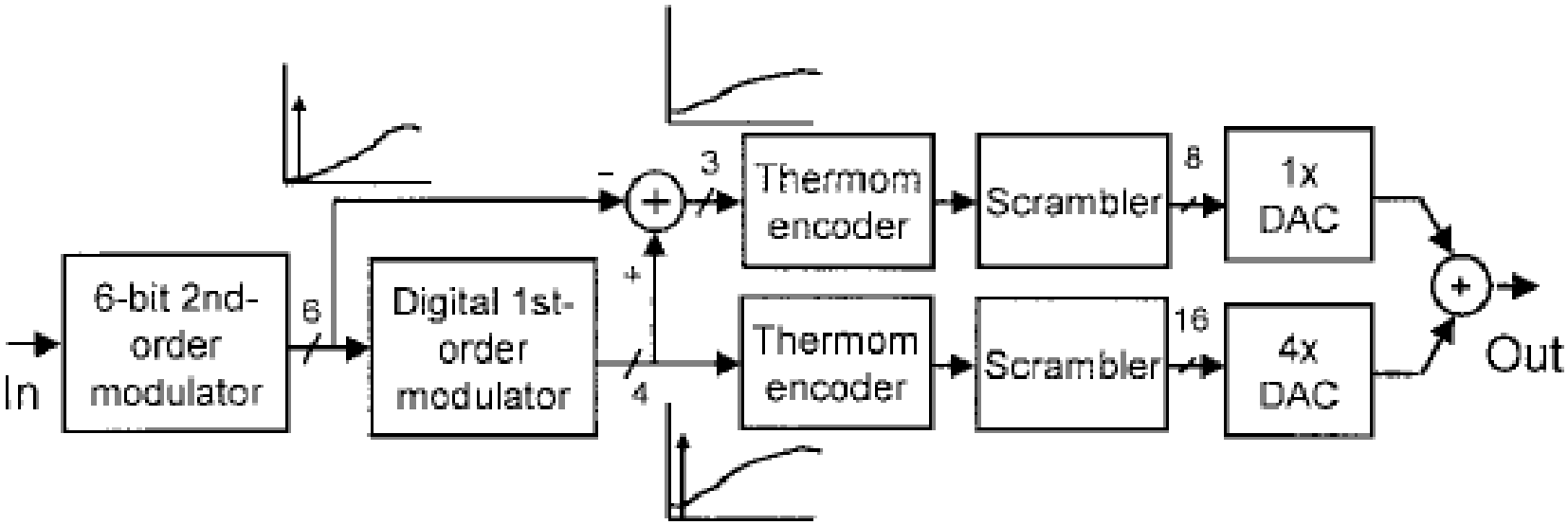
Current Steering ΣΔ-DACs

Segmentation in Oversampling DACs:



Current Steering ΣΔ-DACs

Segmentation in Oversampling DACs:



Current Steering ΣΔ-DACs

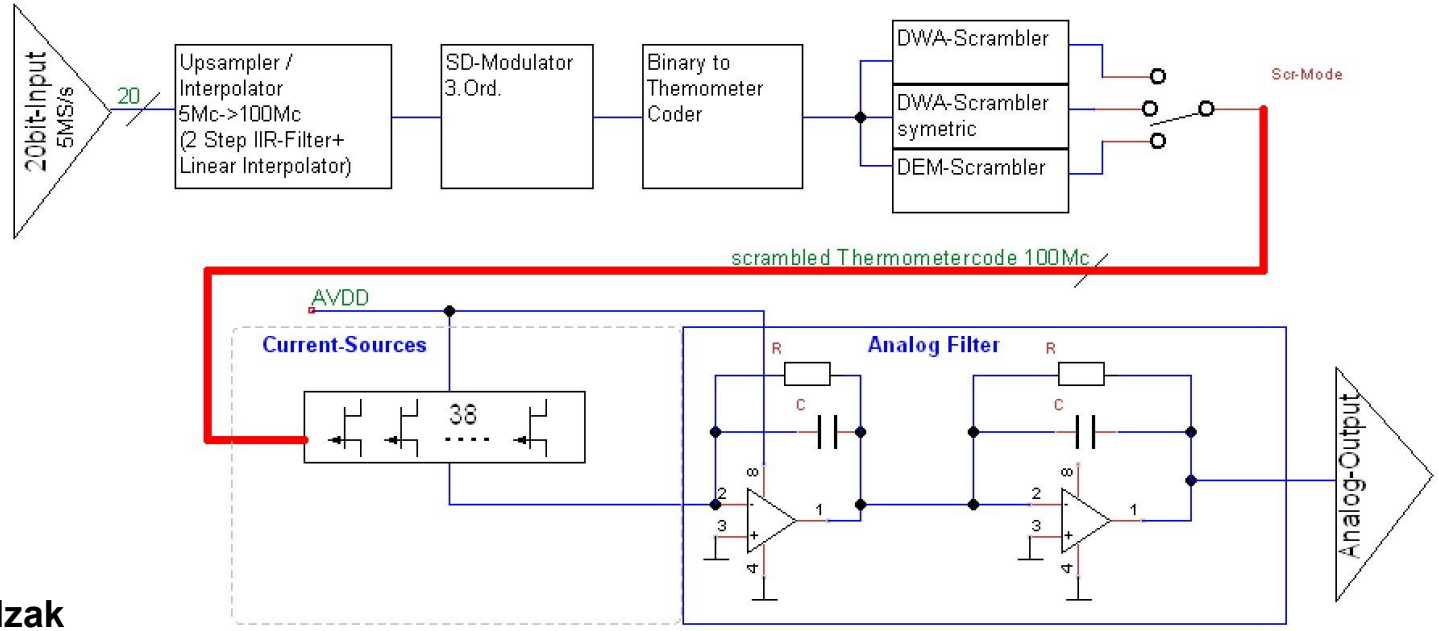
Architecture of 20b linear, 16b noise-free oversampling current-steering DAC with analog filter:

3-stage interpolation: 2x 2x 5x each with digital IIR filter

3th order SD-Modulator, Scrambler (DEM, DWA)

32 current cells => 38 cells to cover overflow issues

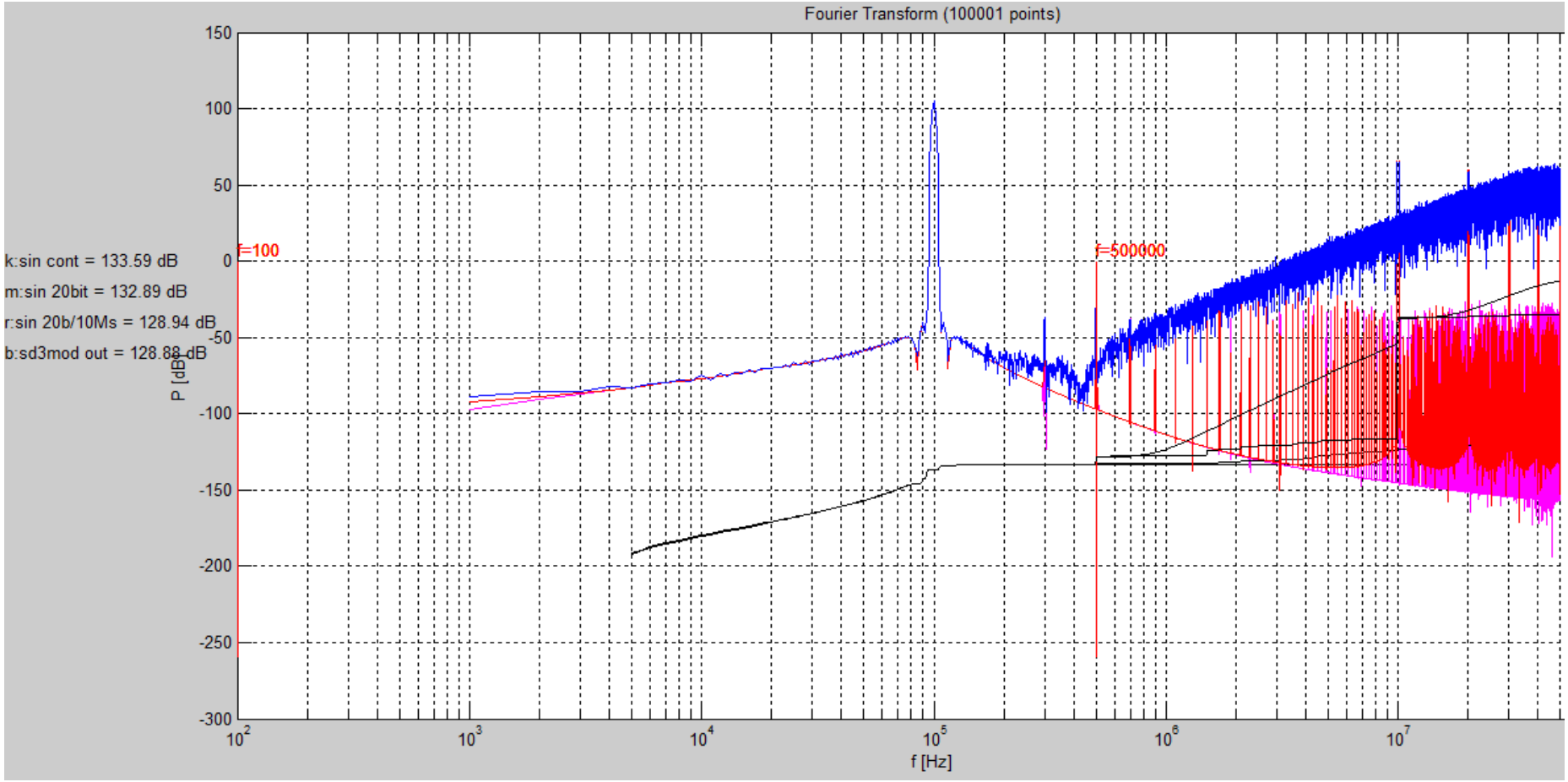
3th order analog RC-filter (1ord TIA, 2ord OpAmp)



Current Steering ΣΔ-DACs

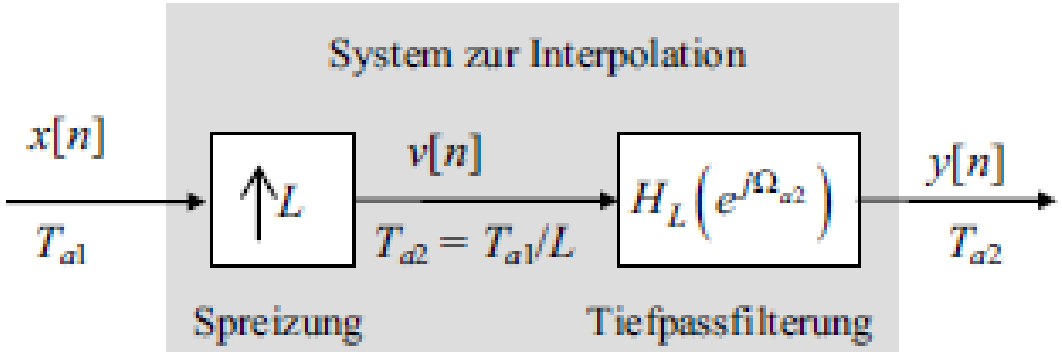
Choosing the right data bit width for each stage: 24b

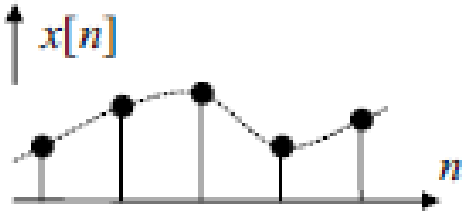
Assessment based on FFT spectrum: distortion (132dB)

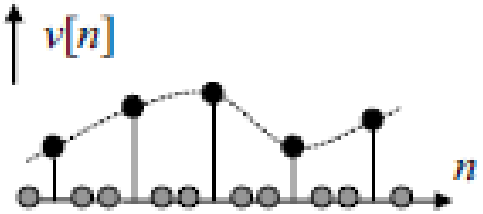


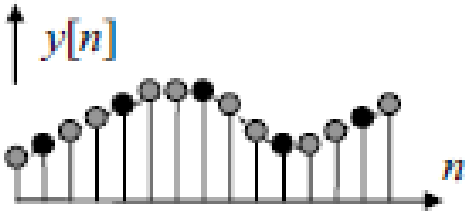
Current Steering ΣΔ-DACs

Interpolation of input data: 10MS/s => 100MS/s



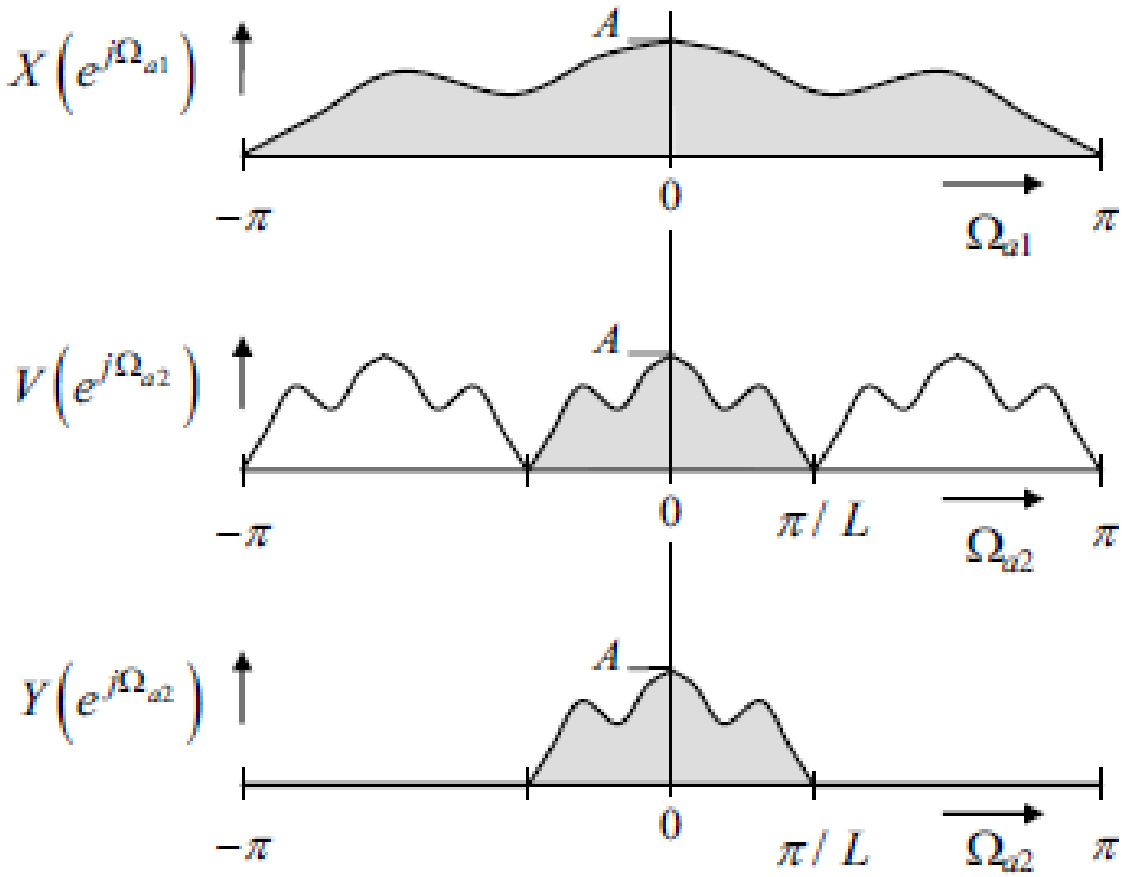






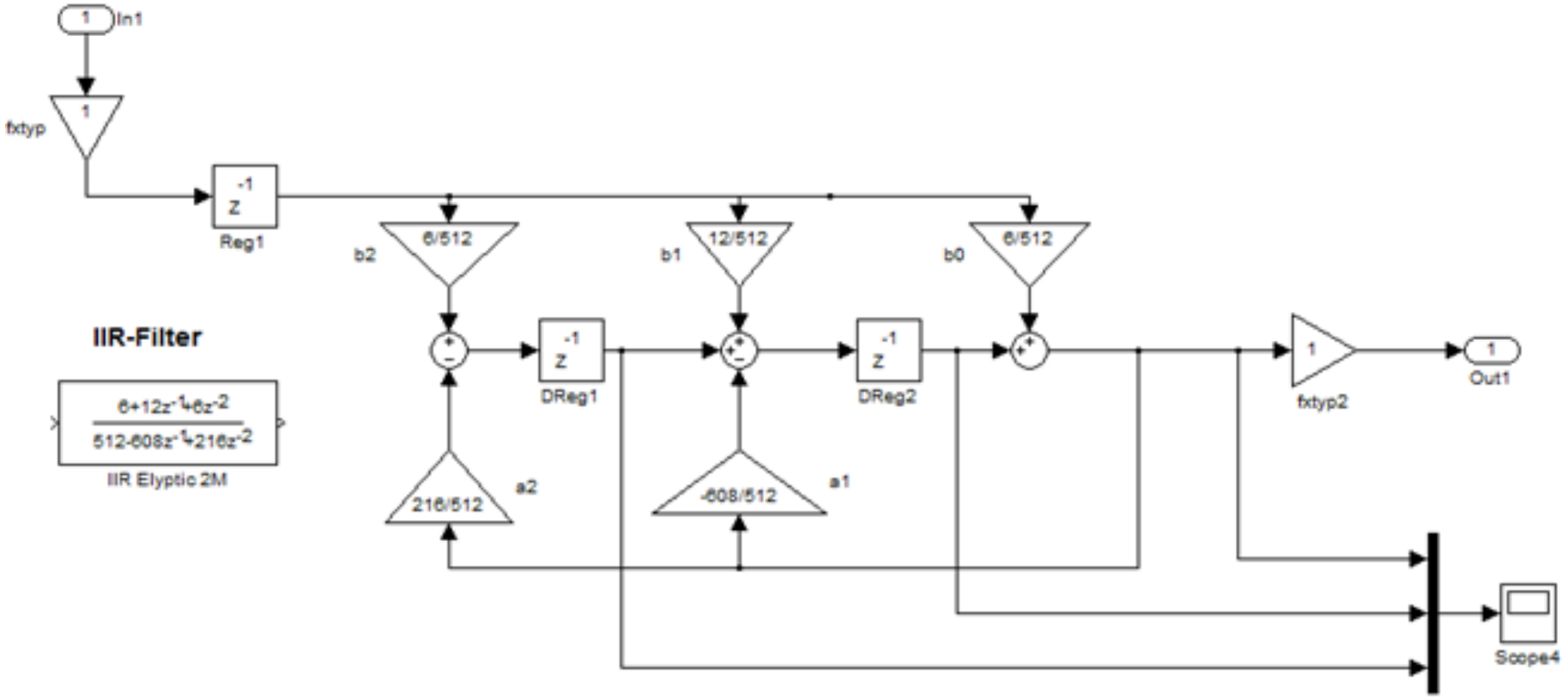
Current Steering ΣΔ-DACs

Interpolation of input data: 10MS/s => 100MS/s



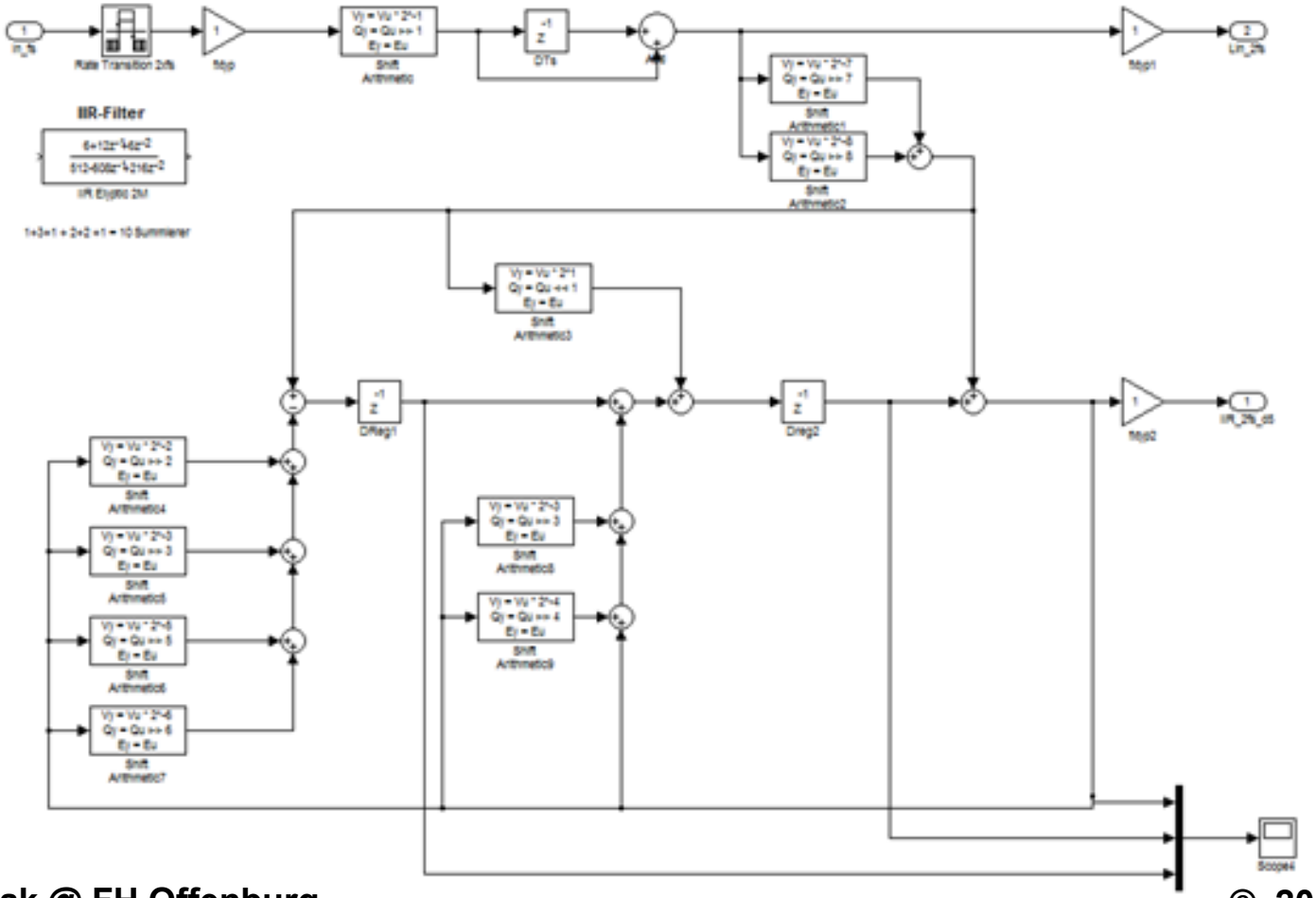
Current Steering ΣΔ-DACs

Interpolation of input data: digital IIR low pass 2nd order filter



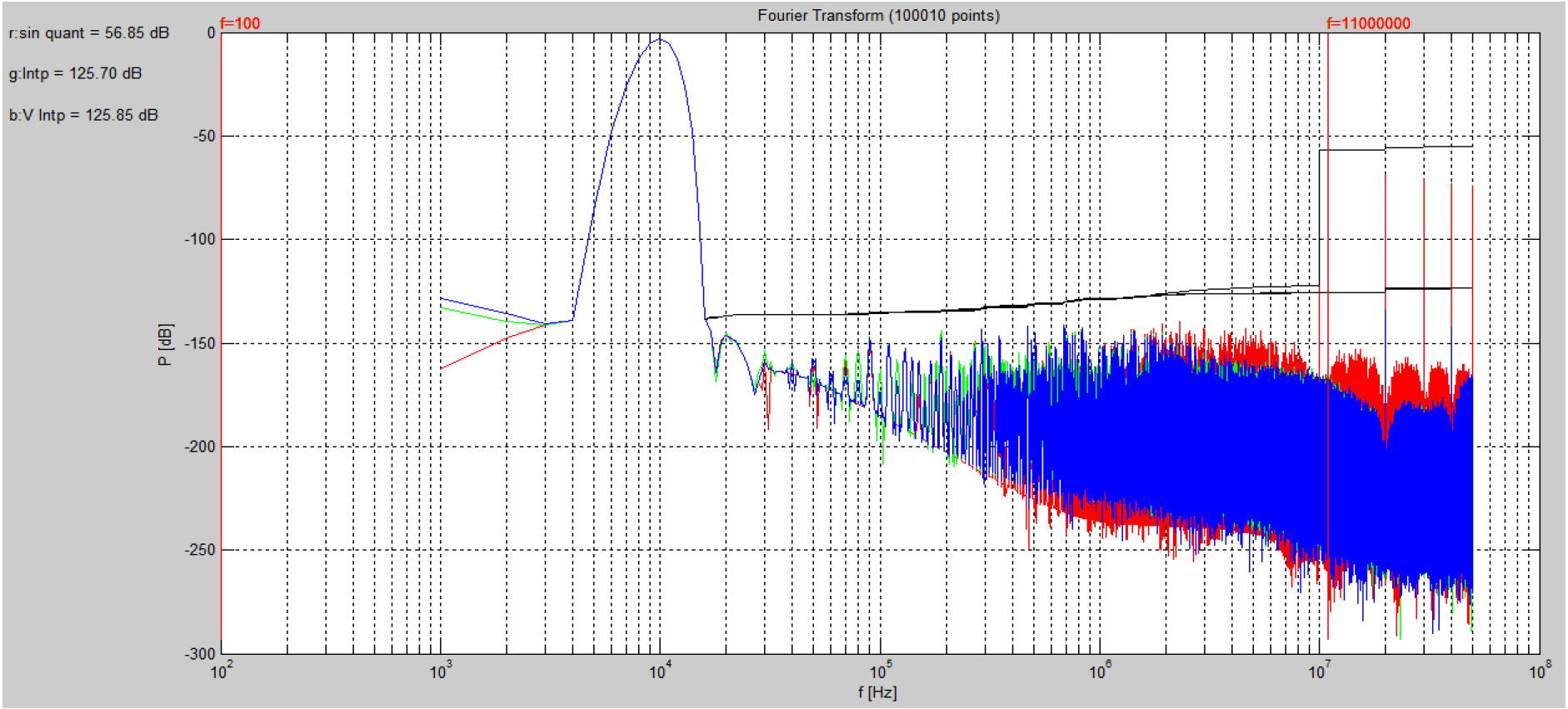
Current Steering ΣΔ-DACs

Interpolation of input data: digital IIR low pass 2nd order filter



Current Steering ΣΔ-DACs

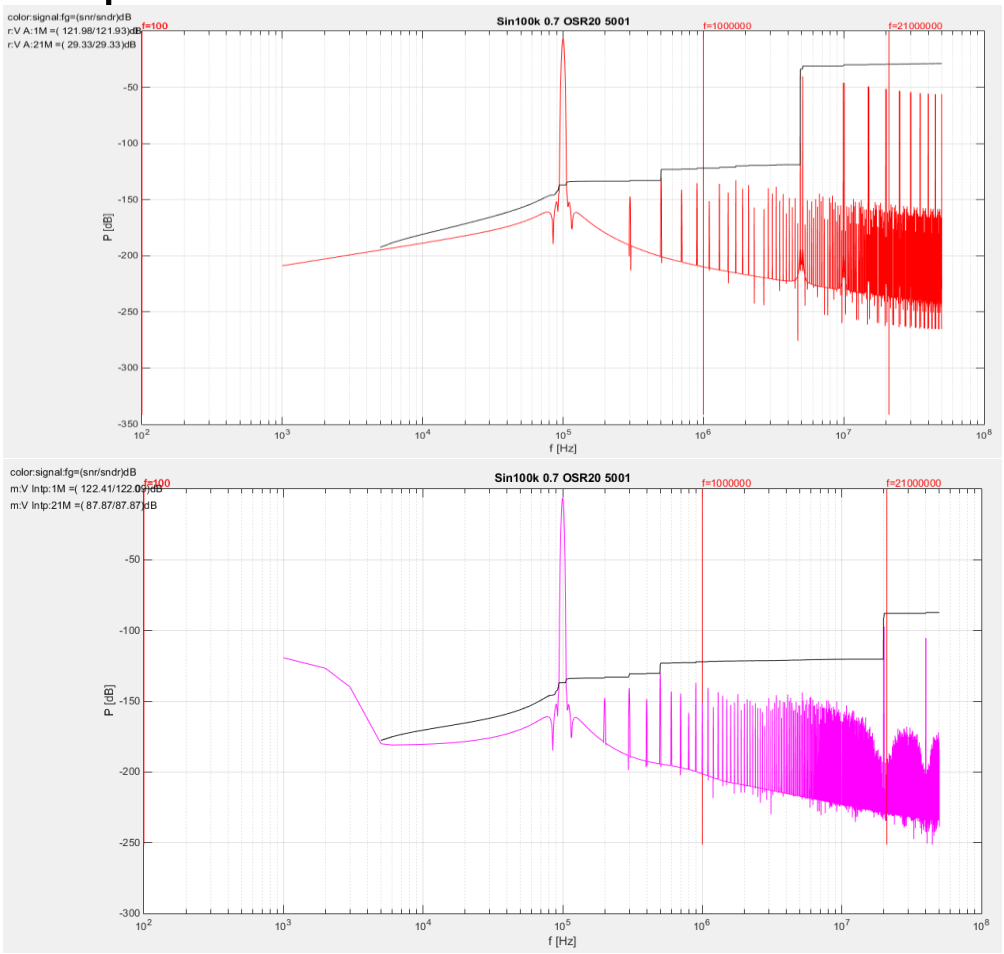
Interpolation of input data: spectral verification



Current Steering ΣΔ-DACs

Interpolation of input data: spectral verification

Interpolator-IIR-Filter Result : Tone Canceling in 4x Upsampling

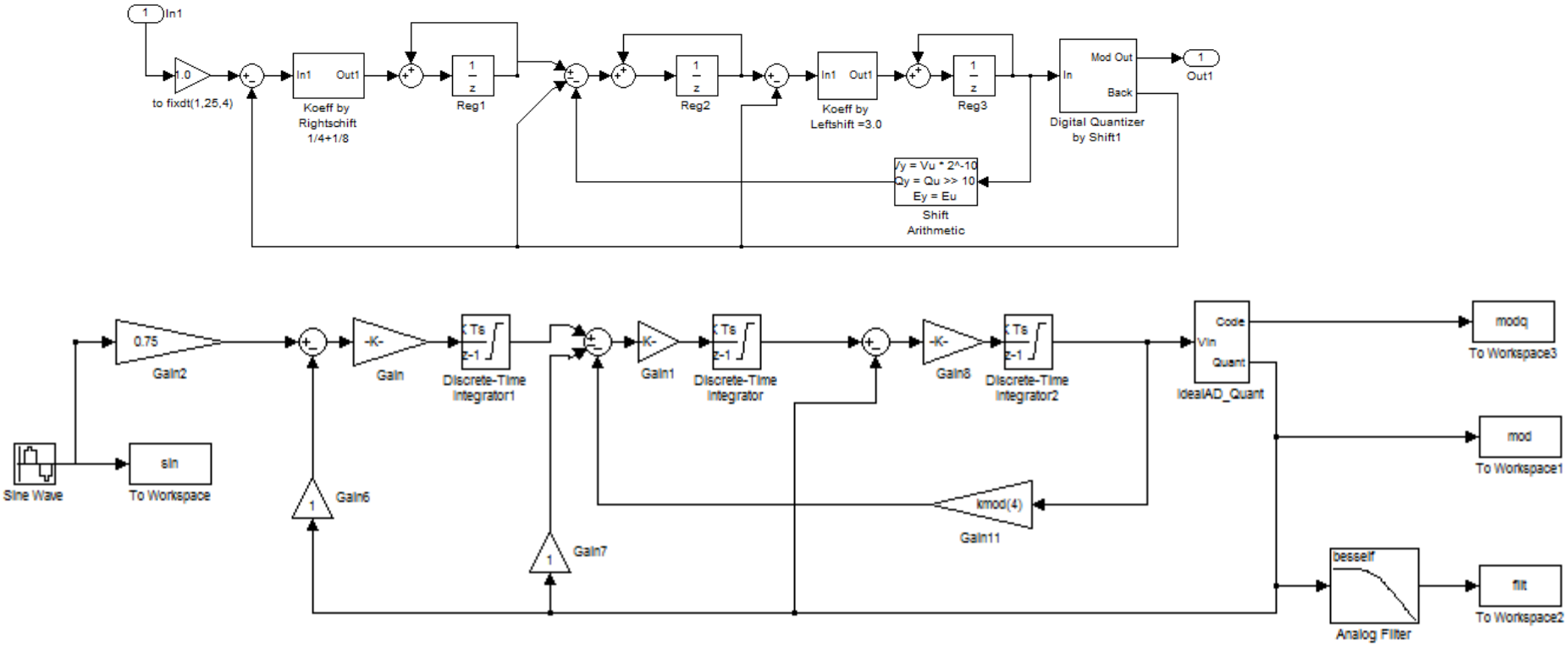


Arising Tones/Spurs
(Distortion)
by Upsampling x4
at 5 and10 MHz
and Multiples Freq.

Canceling Tones
by two IIR dig filters
(2 interpolation stages)
up to 20MHz

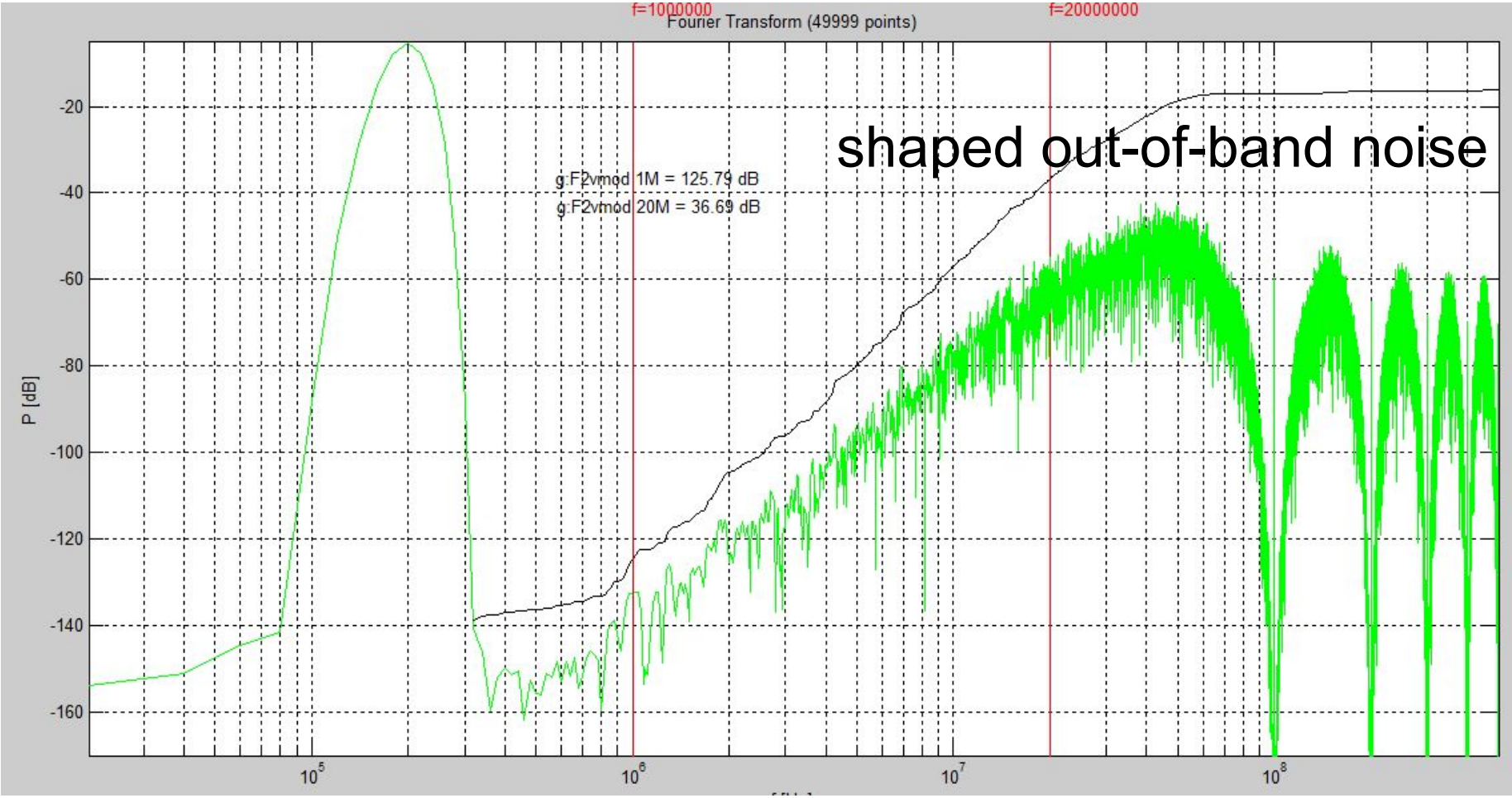
Current Steering ΣΔ-DACs

3rd order Sigma-Delta Modulator



Current Steering ΣΔ-DACs

3rd order Sigma-Delta Modulator: noise shaping

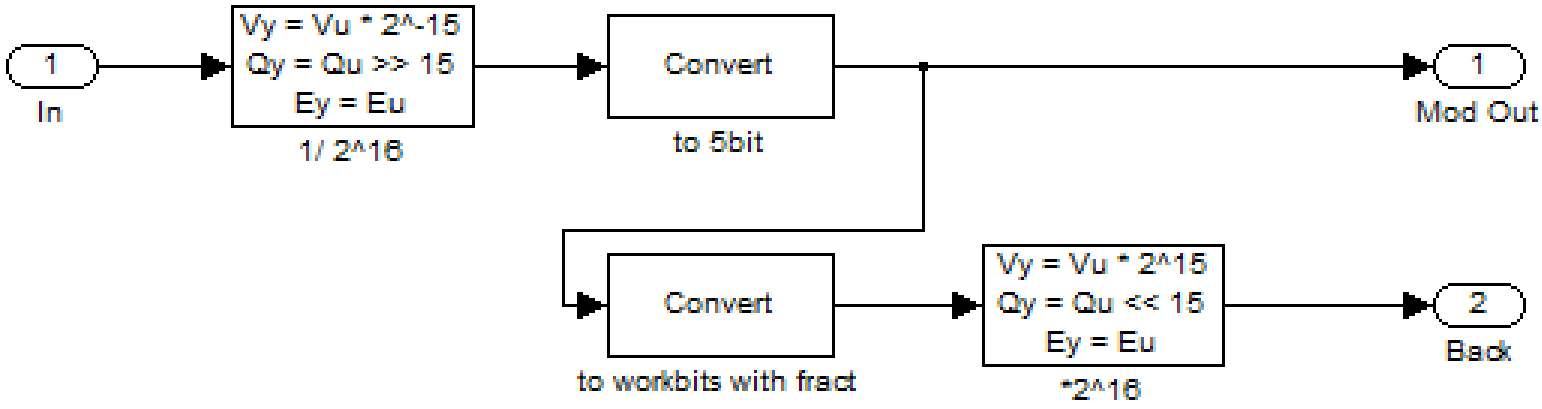


Current Steering ΣΔ-DACs

3rd order digital Sigma-Delta Modulator

- All coefficient (multiplication) have to be realized by Shift-and-Add operation (circumventing true multipliers)

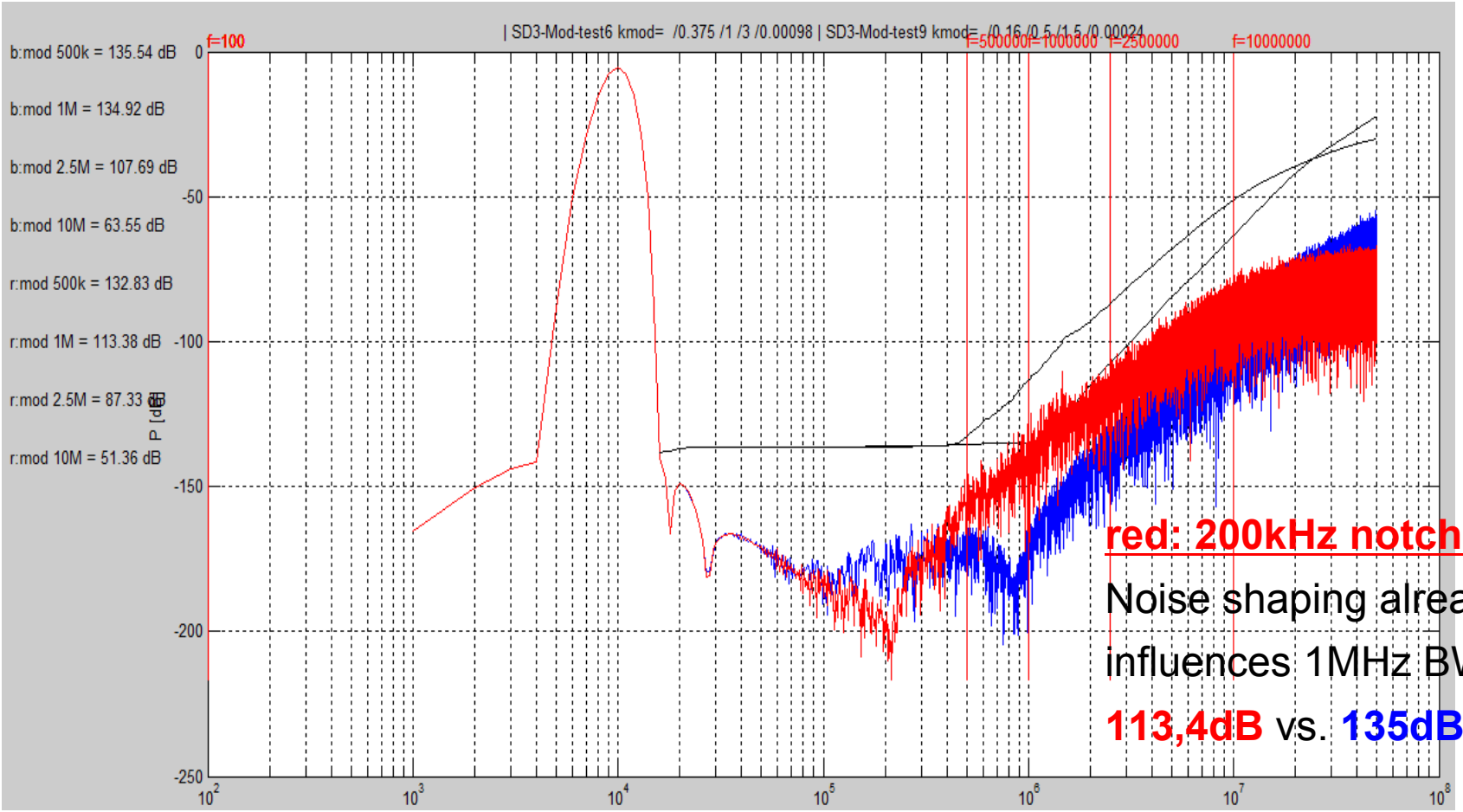
- Cascade of adders should not limit the delay for the 10ns clocked operation



Current Steering ΣΔ-DACs

3rd order Sigma-Delta Modulator

- notch optimization/shift for lowest in-band noise



Scrambler

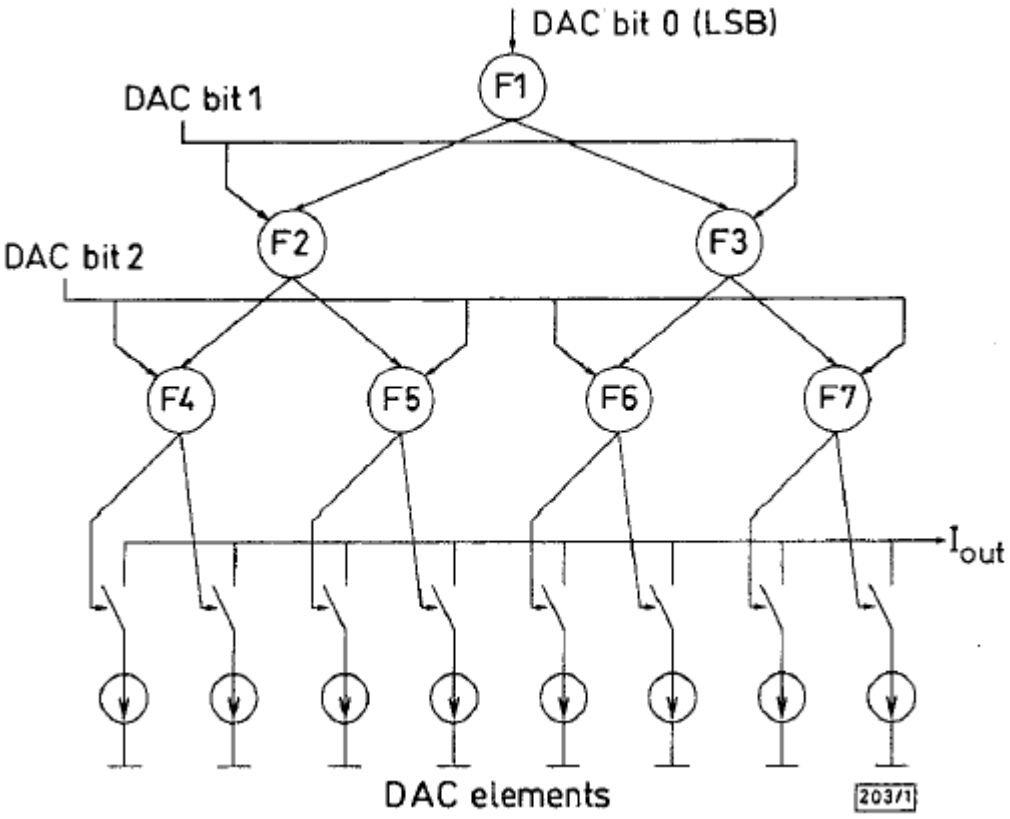
When a certain cells shows a mismatch of 2%, while activating this cell causes distortion.
When the activation of this unique cell is randomized , the distortion is interchanged for noise. (THD↓, SNR↑)

Scrambler / Randomizer is used to select certain current cells when each of the 32(38) bits are active. There are different algorithms implemented:

- 4- or 5-level DEM (dynamic element matching)
- DWA (data weight averaging) over the whole array
- Splitting array into half: symmetrical DWA

Scrambler

3-level DEM (Dynamic Element Matching)



Scrambler

3-level DEM (Dynamic Element Matching)

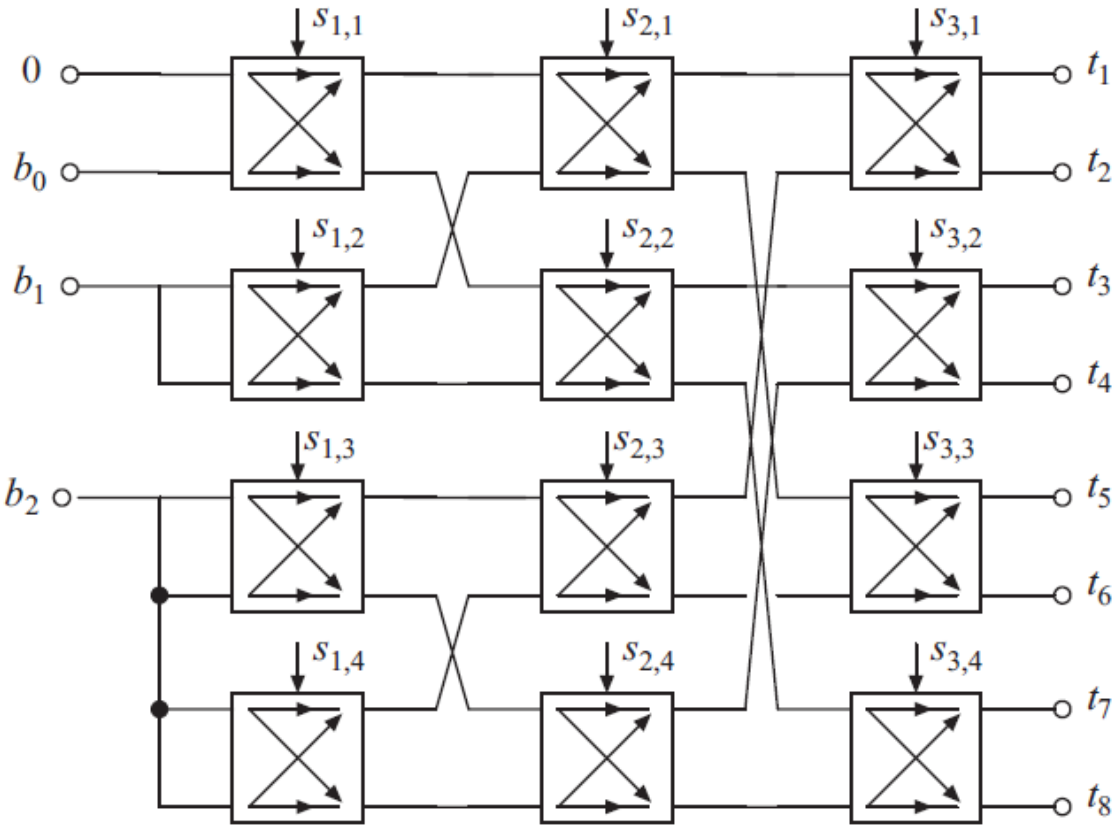
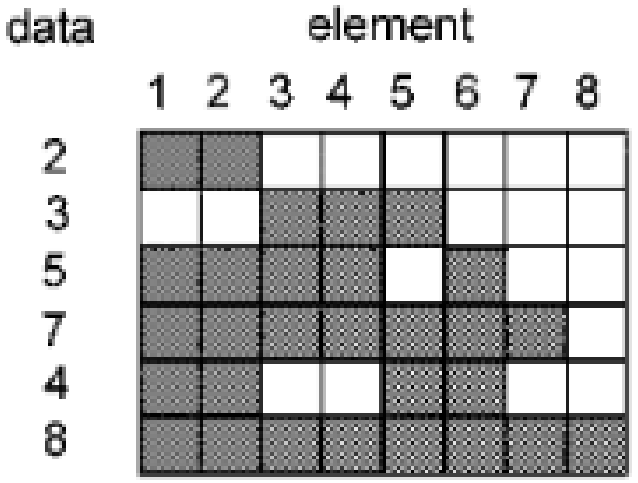
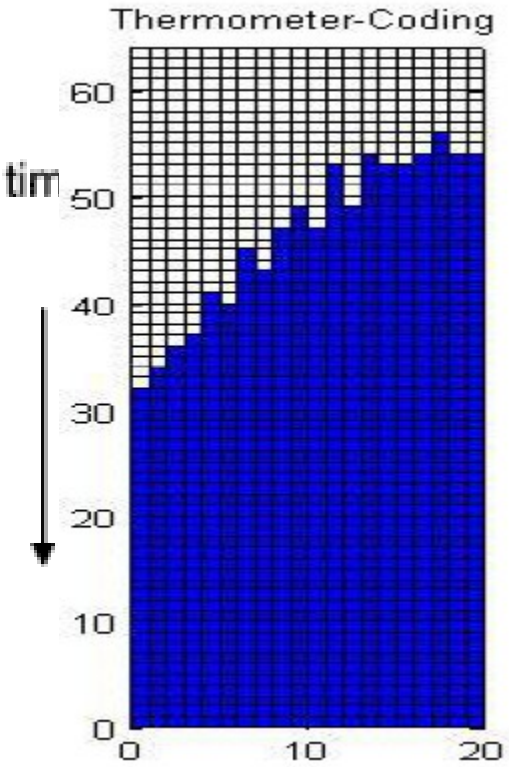


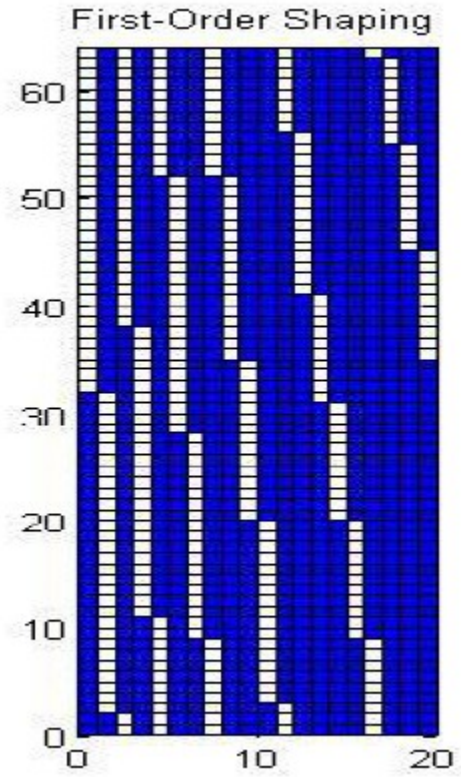
Figure 7.14 Segmentation and scrambling 3-to-7 binary-to-thermometer encoding circuit implemented by a GCN.

Scrambler

DWA (Data Weight Averaging): instead of current cell activation from initial point, a vector shows which cell has been used last time







Scrambler

DWA (Data Weight Averaging): beside of init point vector, each time also the direction is reversed

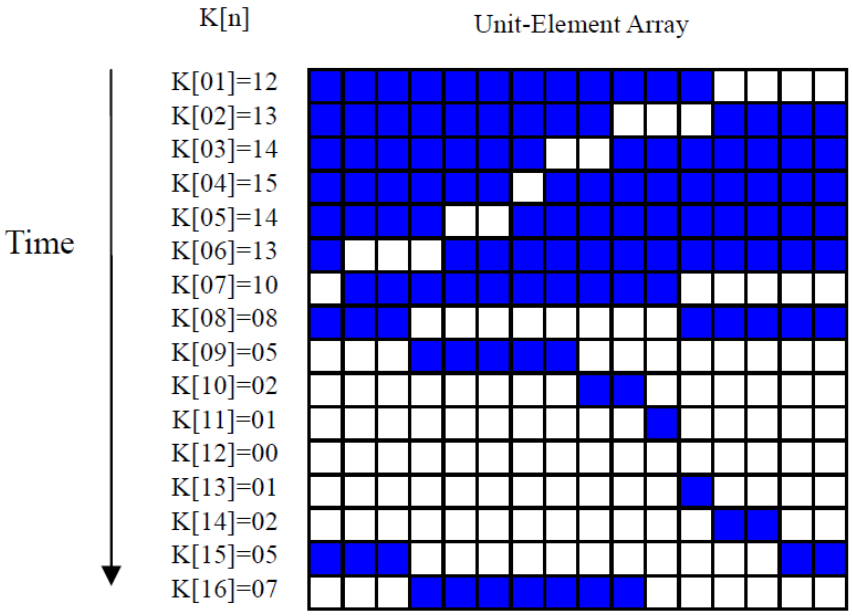


Figure 18. The DWA operation principle

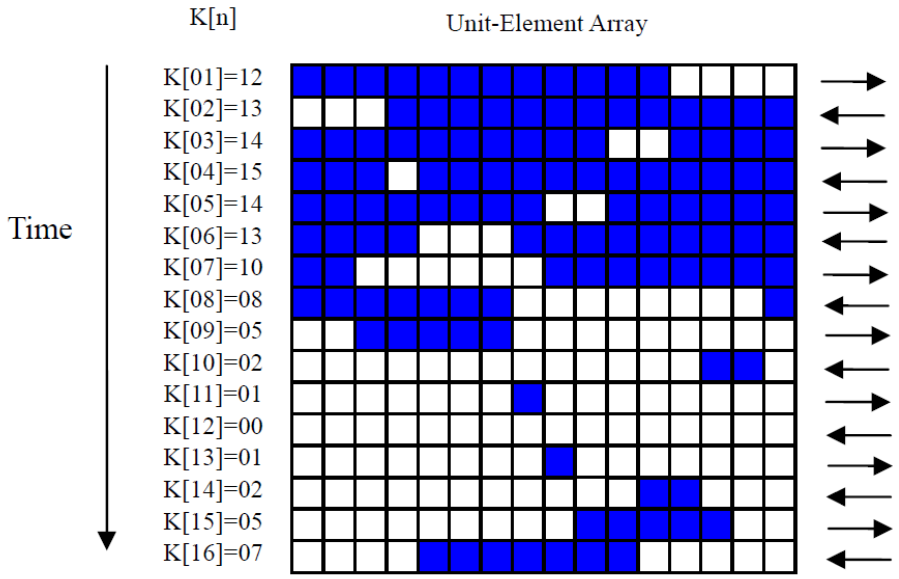
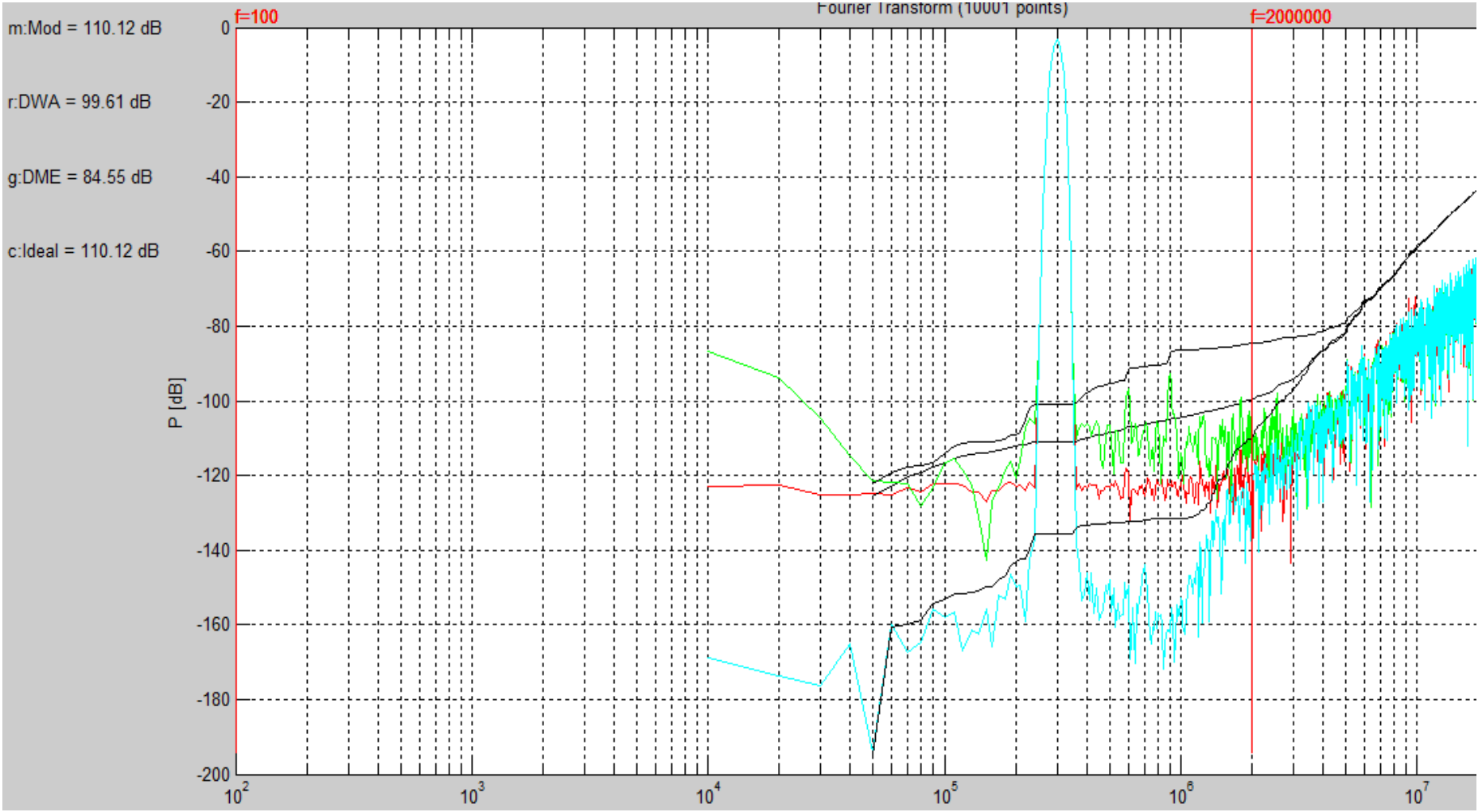


Figure 25. The Bi-DWA operation principle.

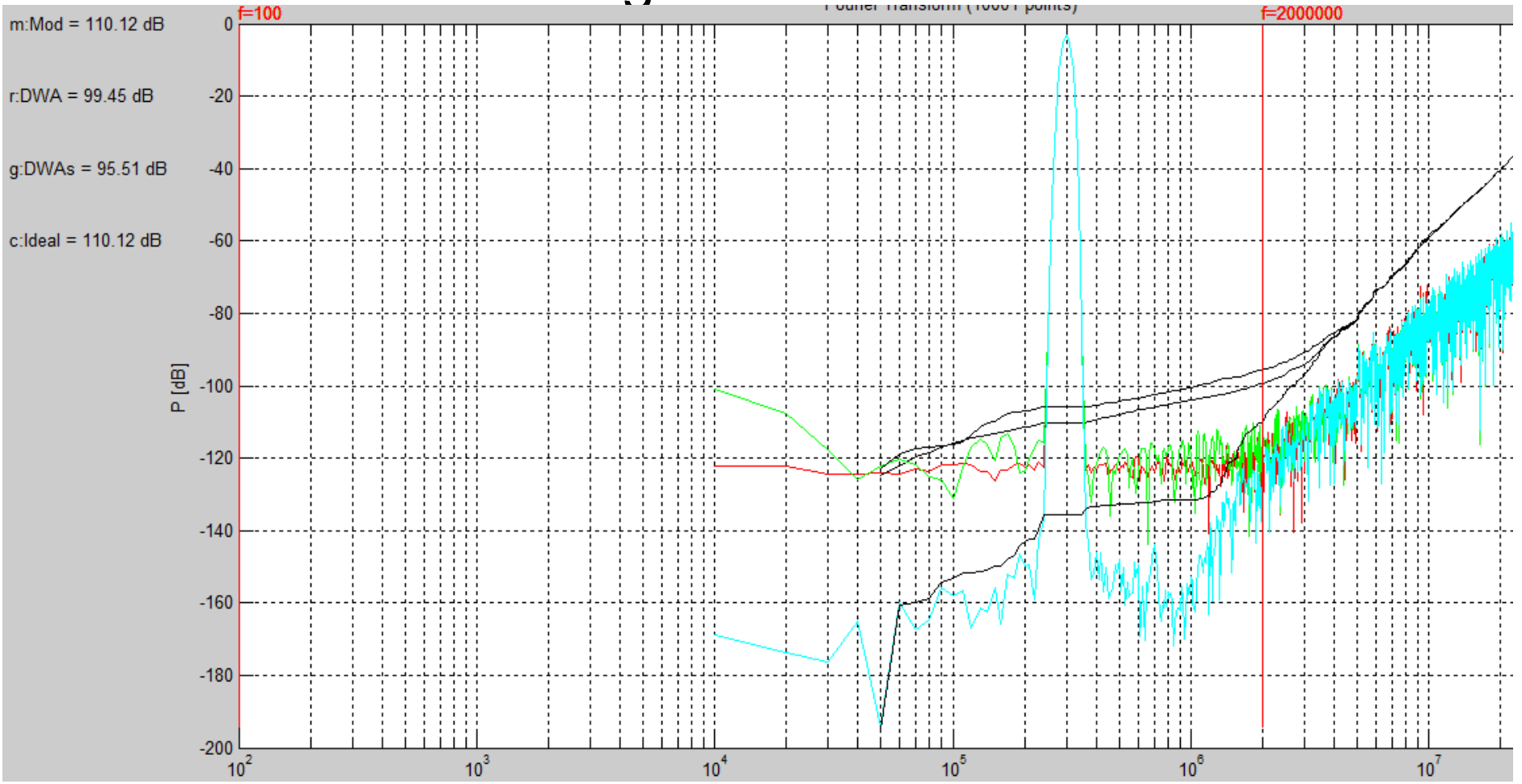
Scrambler

Spectral verification: DEM vs. DWA algorithm



Scrambler

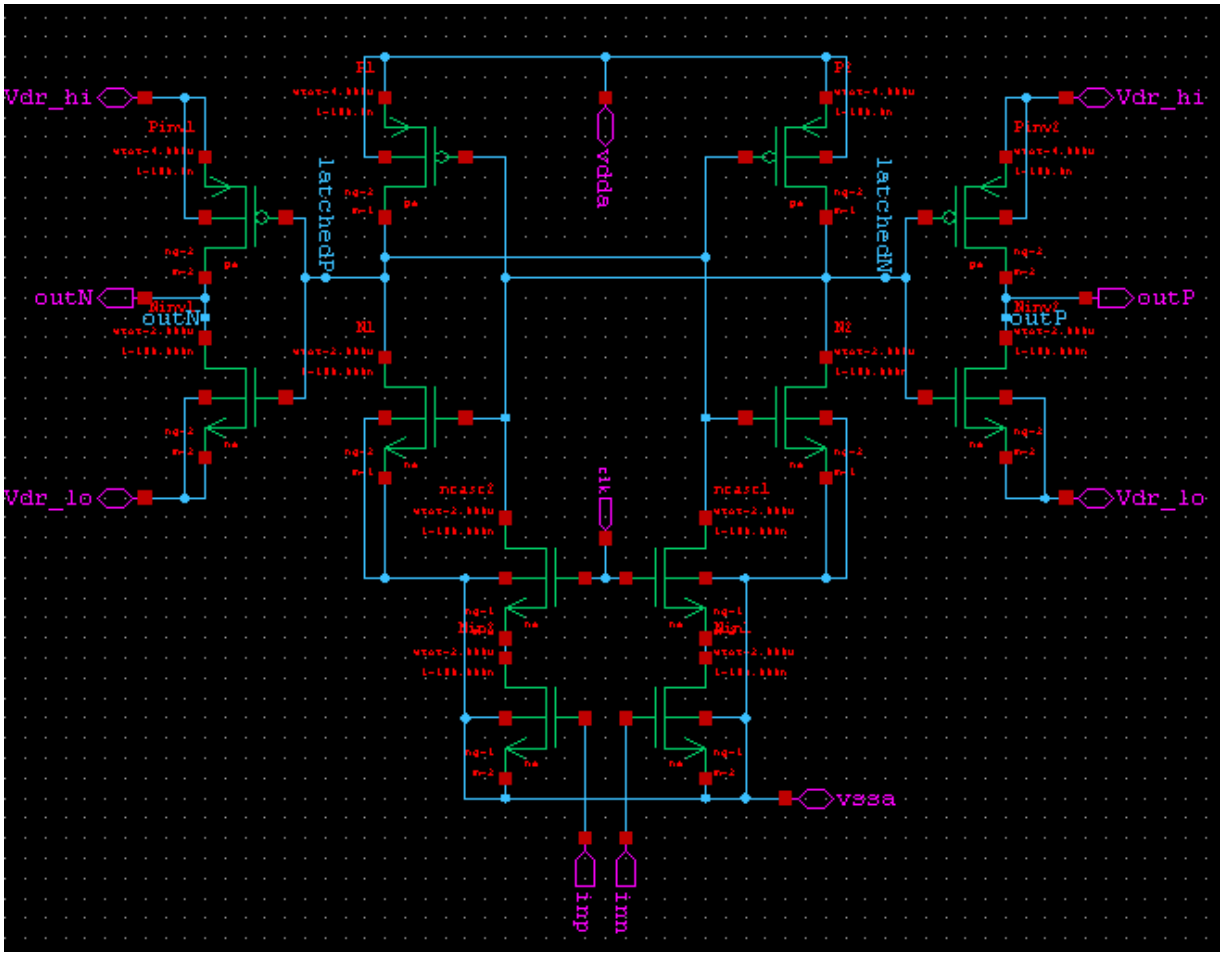
Spectral verification of DWA algorithms:
1% mismatch in analog current cell model



Current Steering ΣΔ-DACs

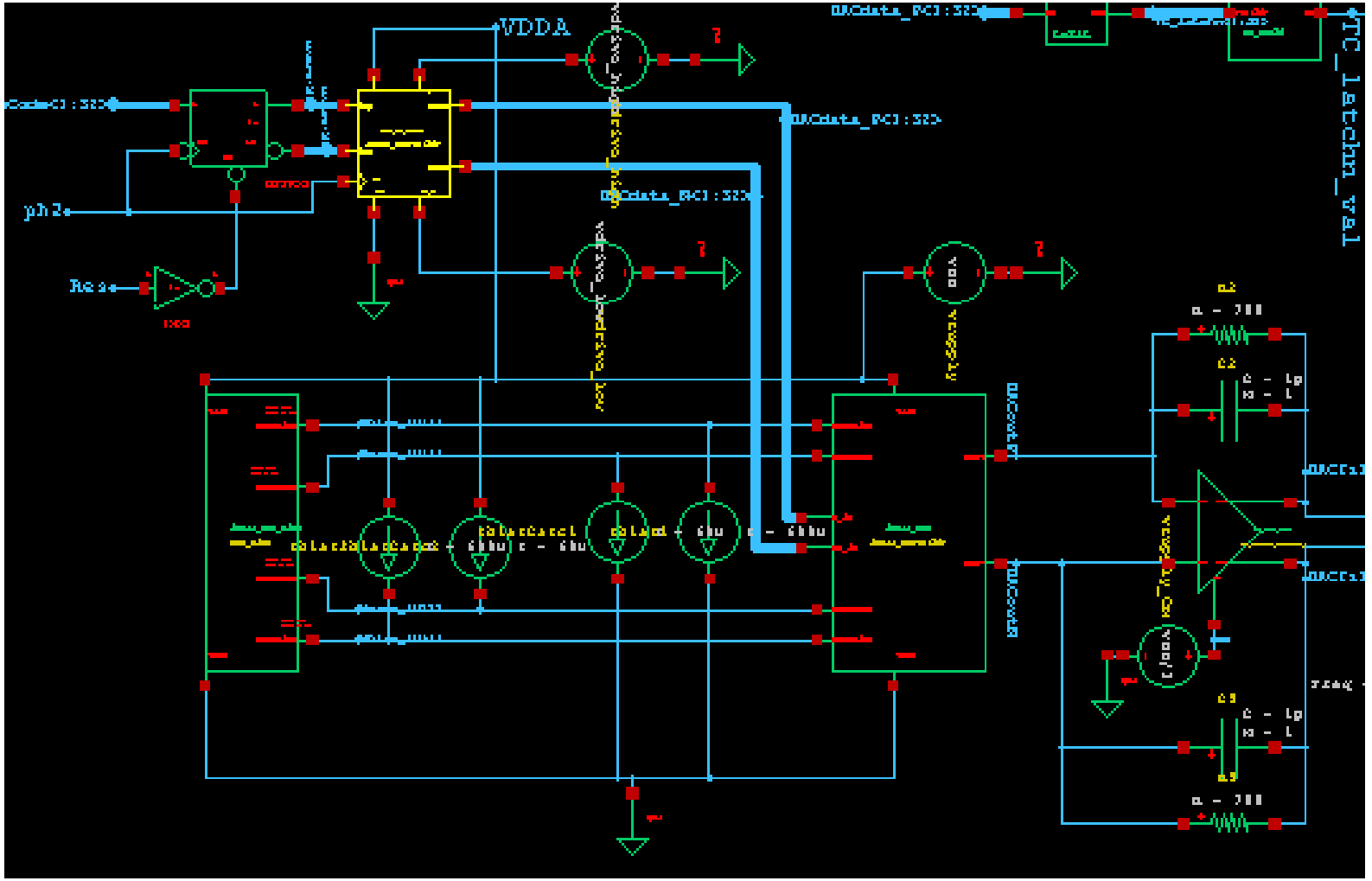
Analog-to-Digital Interface: Curret cell driving latches:

hiCross driver for NMOS / lowCross for PMOS sources



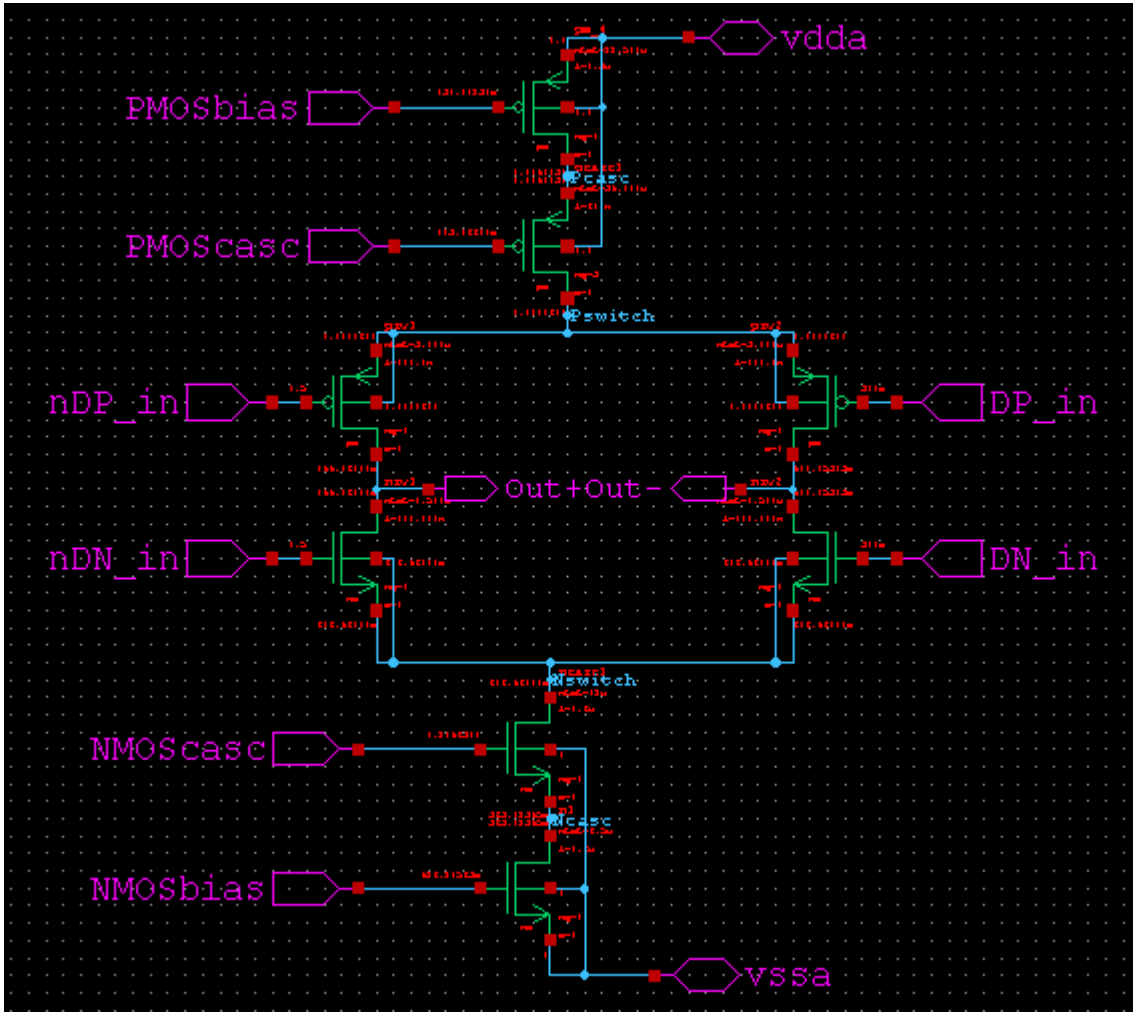
Current Steering ΣΔ-DACs

Analog-to-Digital Interface: Cell driving latches & current cells



Current Steering ΣΔ-DACs

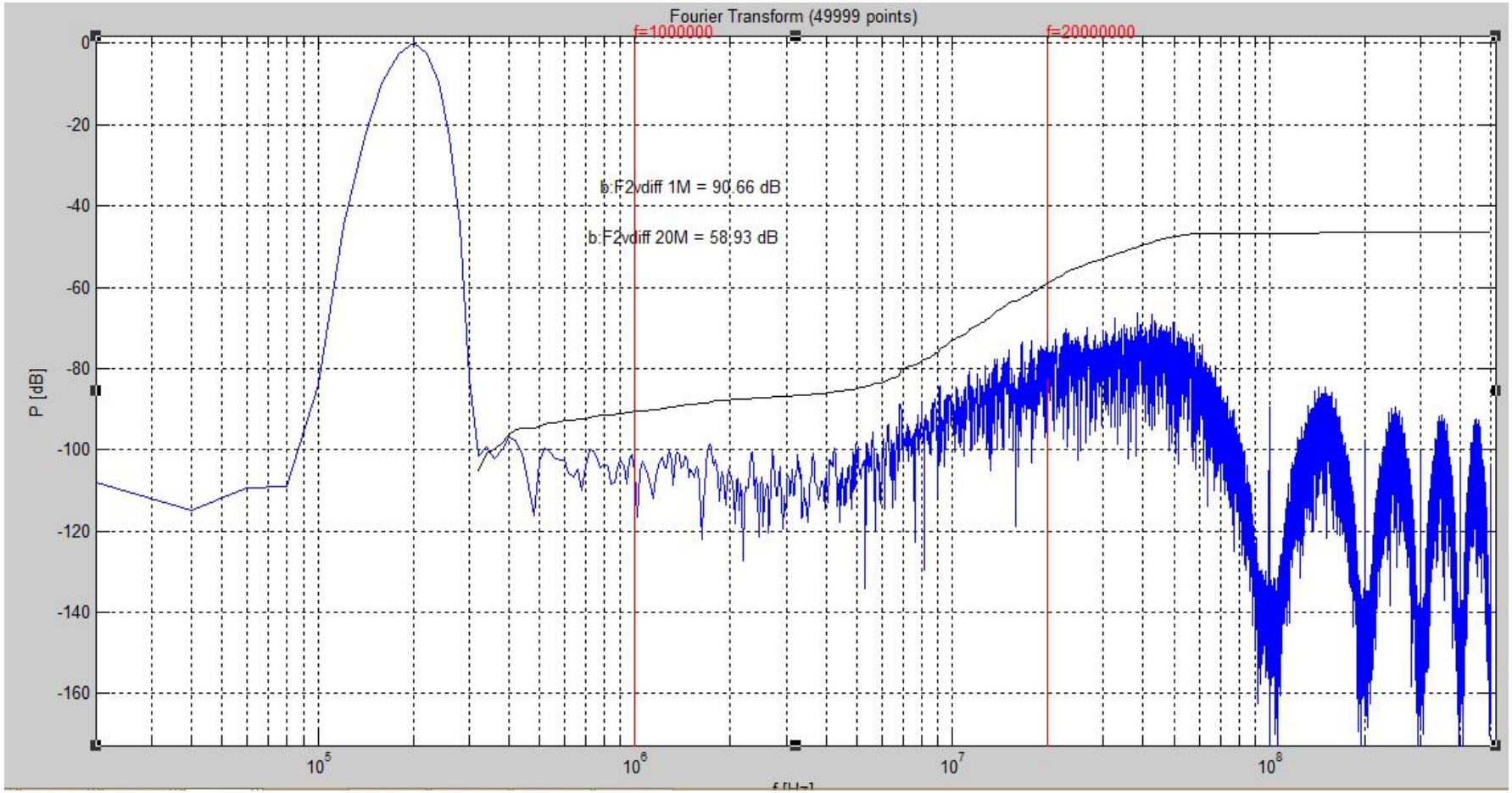
Analog Circuit Block: Complementary Cascode Current Cells



Current Steering ΣΔ-DACs

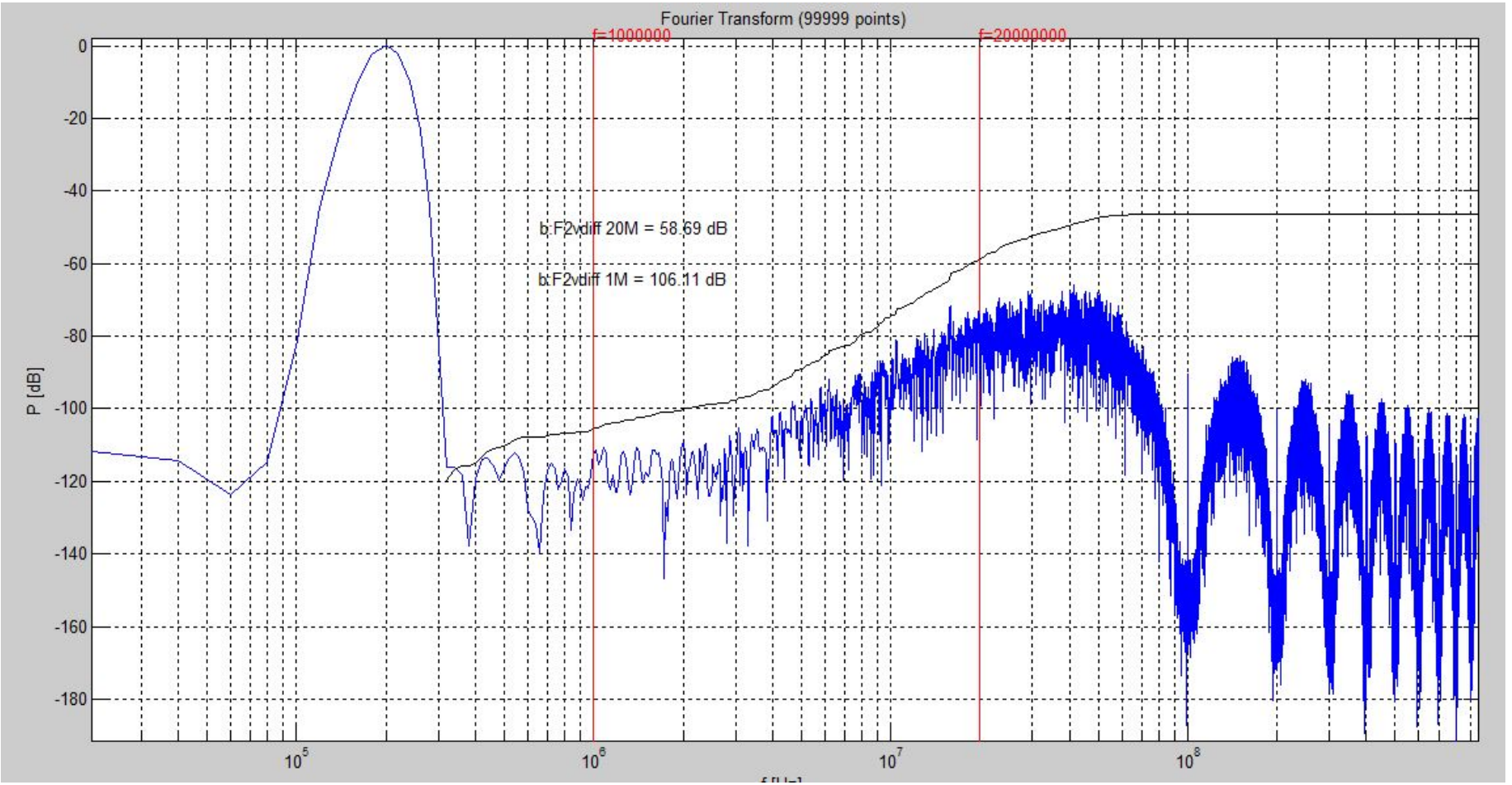
Spectral verification: SPICE simulation sampled into file.

Post-processing in a FFT Script in Matlab: SNDR integration



Current Steering ΣΔ-DACs

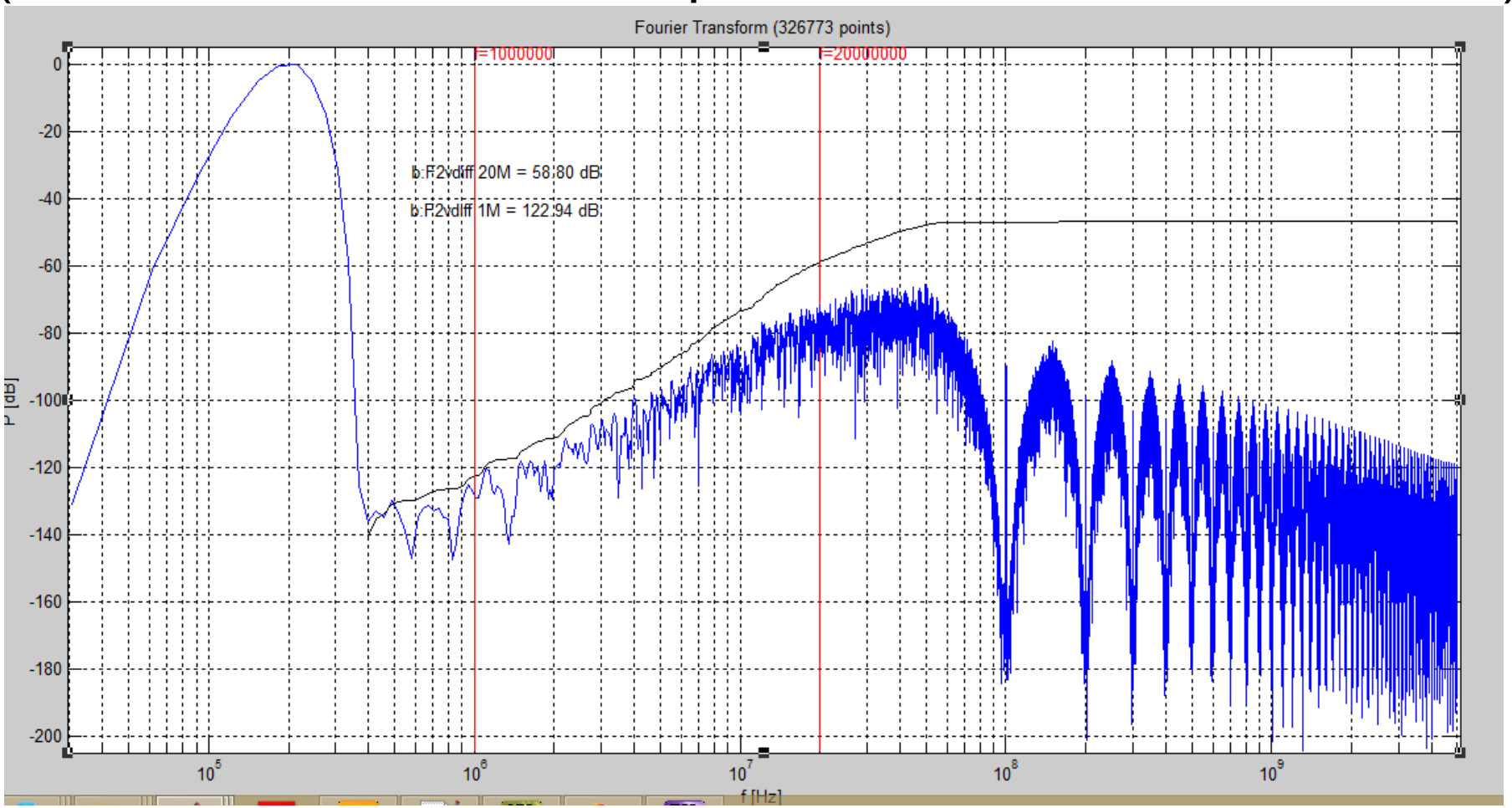
Spectral verification: ideal latches with Hi/Lo crossing (ideal overtaking of current cell between NMOS-PMOS)



Current Steering ΣΔ-DACs

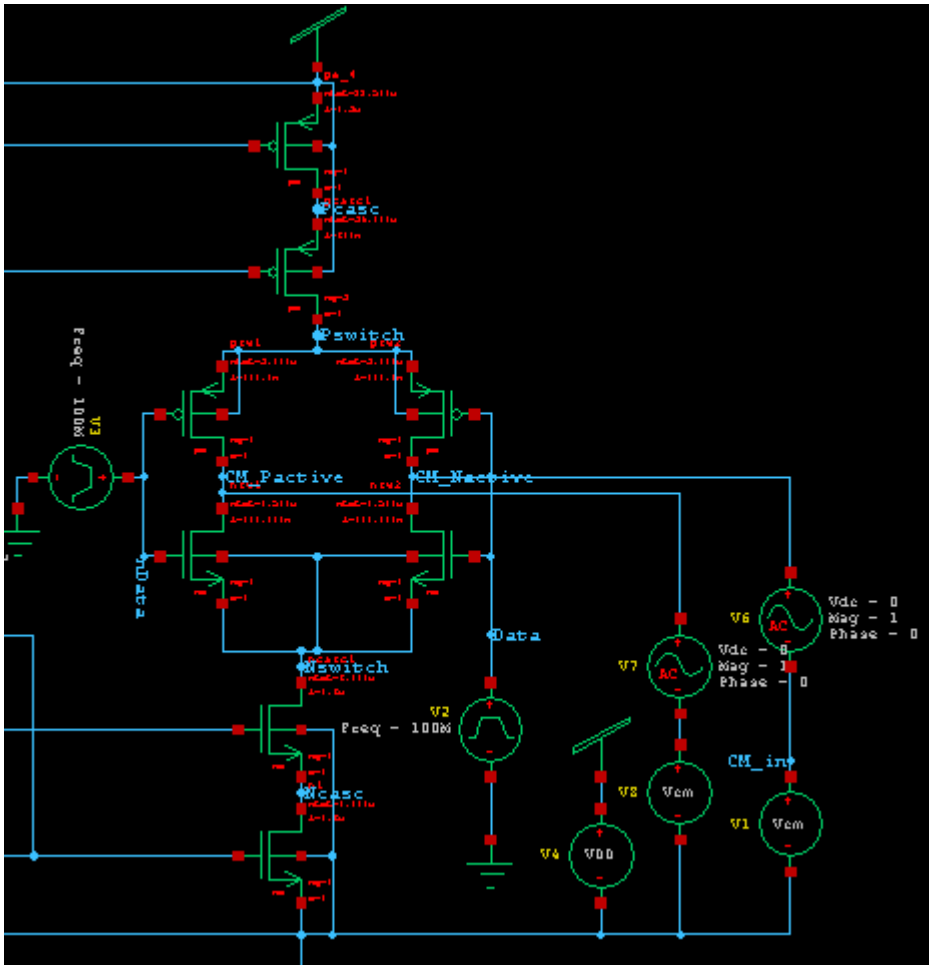
Spectral verification: ideal NMOS curr. source, real PMOS:

(influence of the limited output resistance of P-current cells)



Current Steering ΣΔ-DACs

Output impedance of the NMOS/PMOS cells

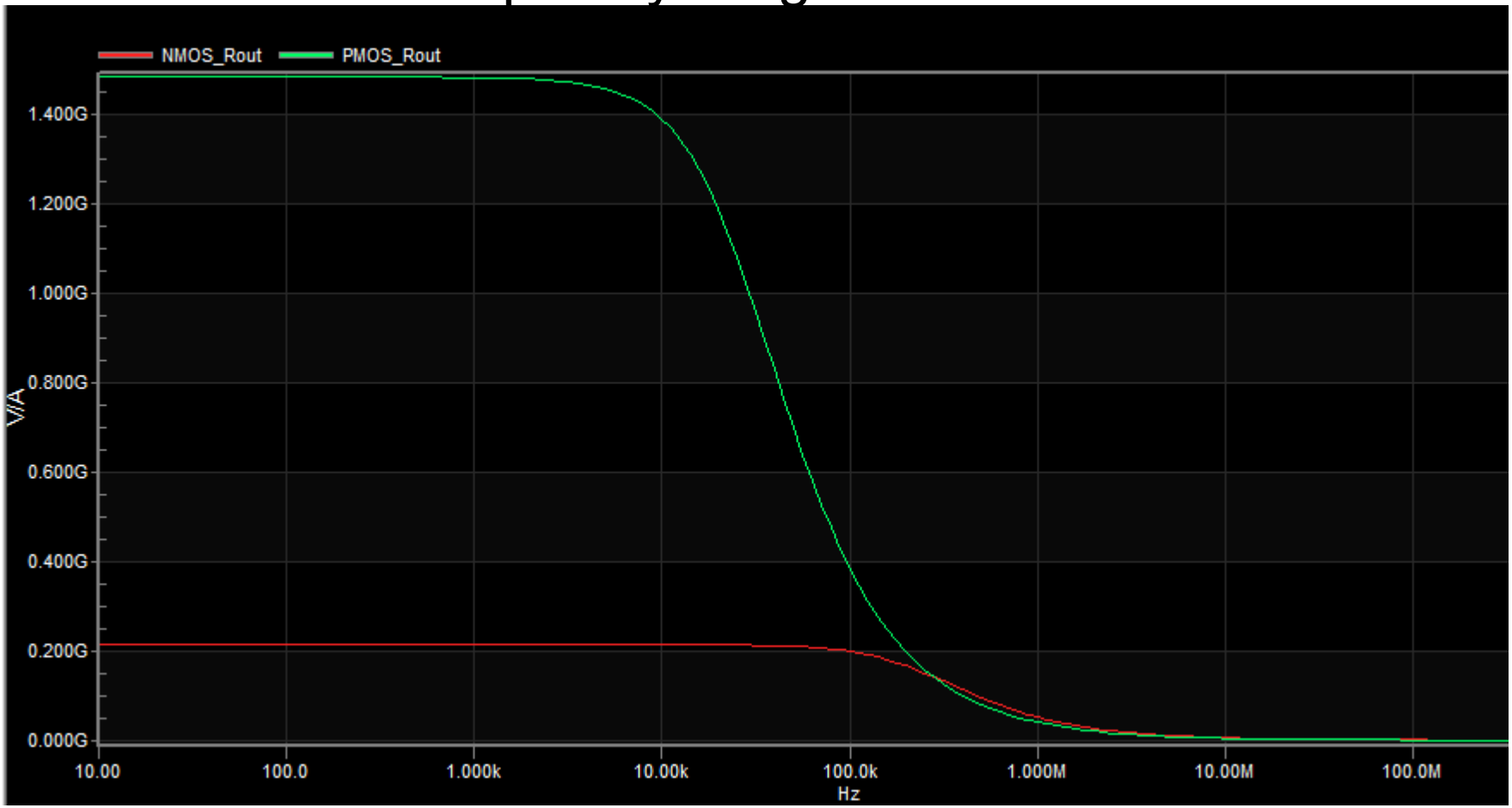


SPICE Test bench: Fixing the switch to a certain position: left NMOS on, right PMOS on

V-AC stimulation from the output node

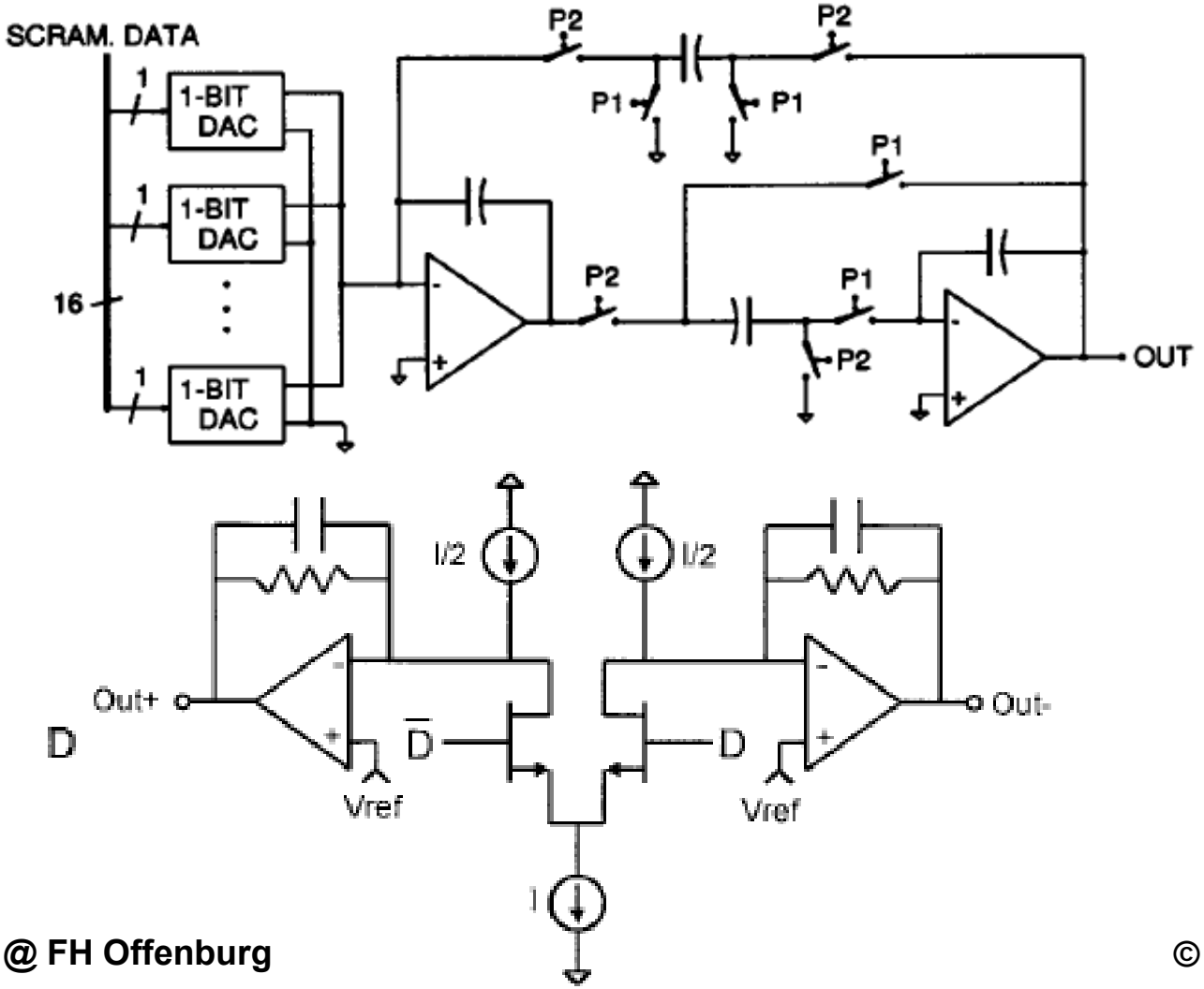
Current Steering ΣΔ-DACs

Output AC impedance of the NMOS/PMOS cells vs. frequency range of the DAC



Current Steering ΣΔ-DACs

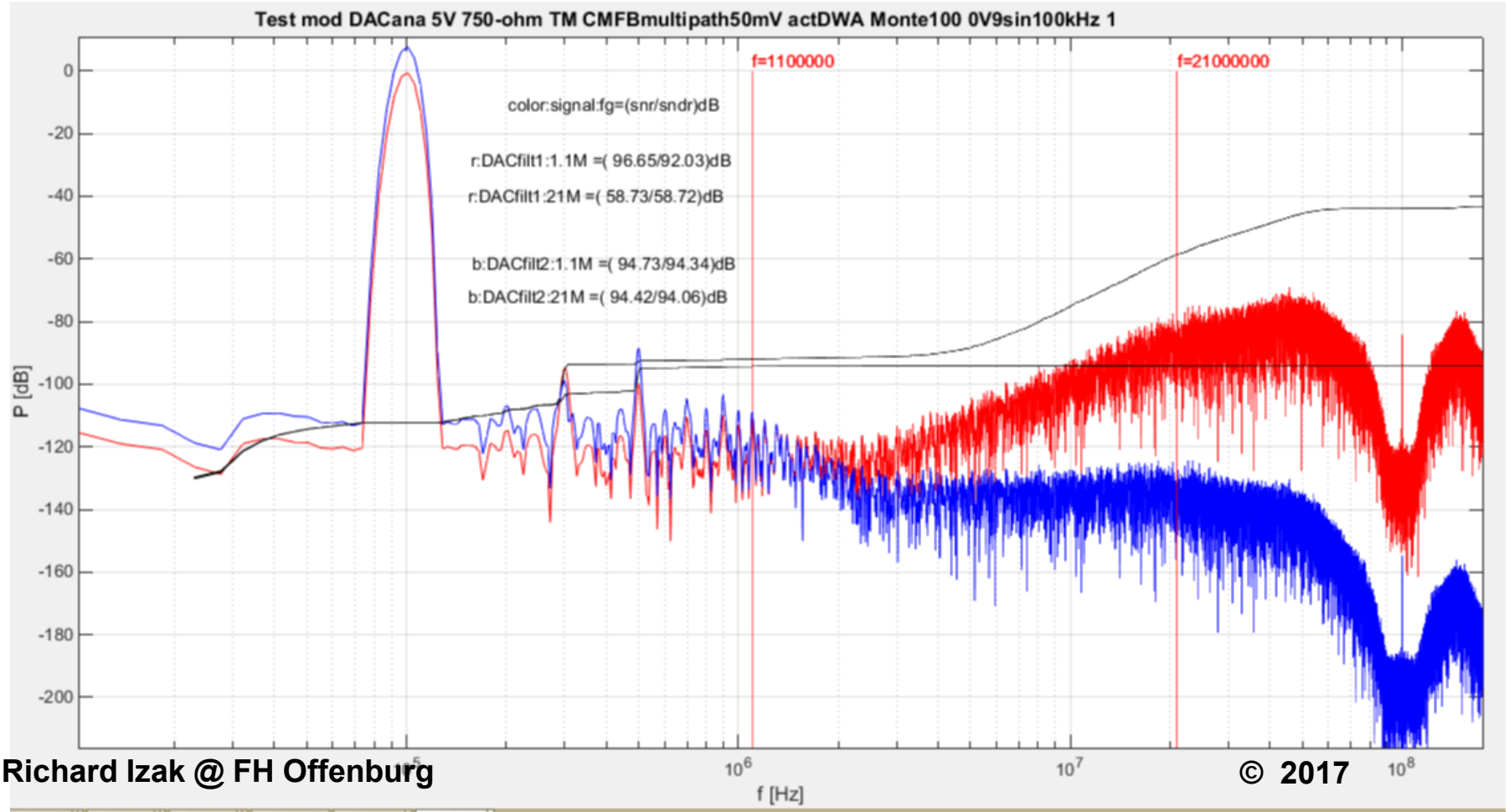
Analog Reconstruction Filtering: SC or activeRC



Current Steering ΣΔ-DACs

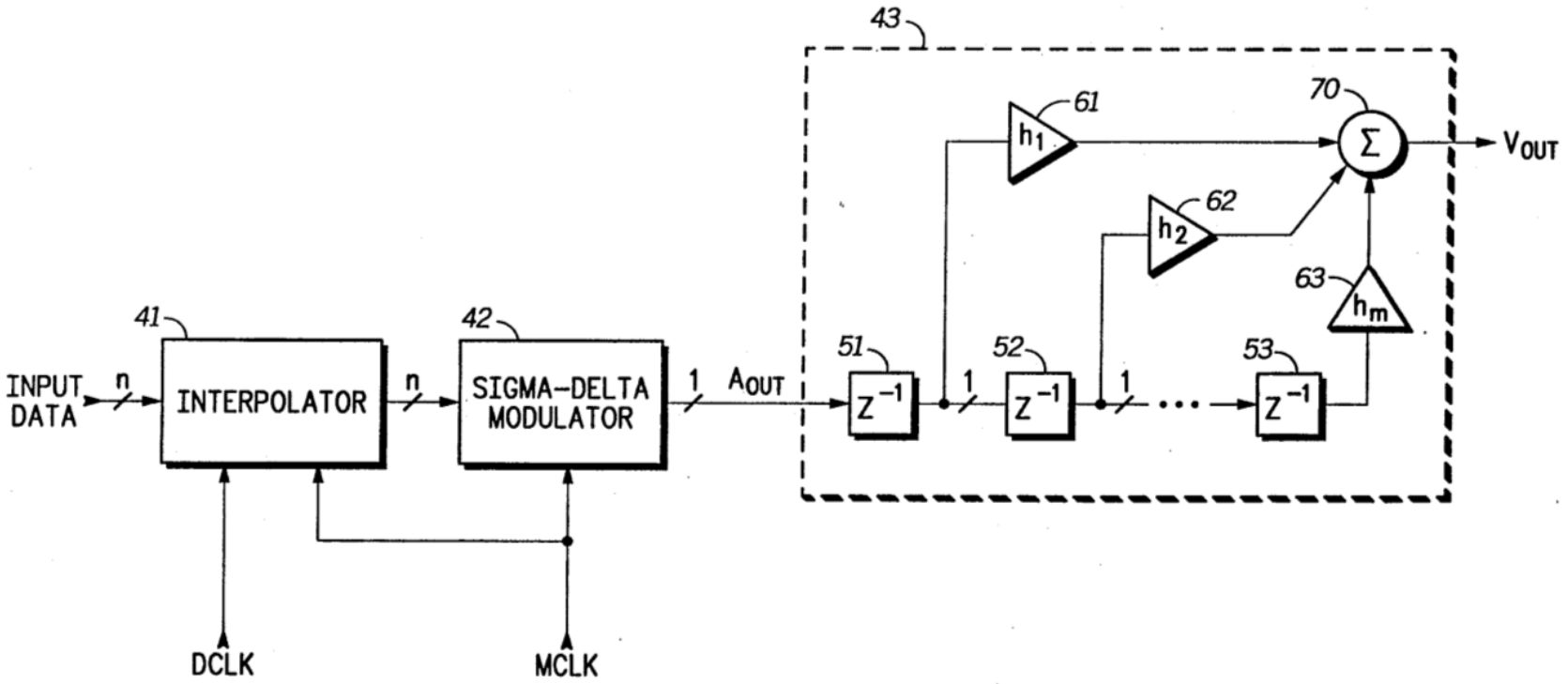
Spectral verification: SD-DAC with current cell MC-mismatch and scrambler DWA/DEAM enabled; **Red: :** ∑Δmod & analog current cells (MC mismatch)

Blue: ∑Δmod & current cells & 3ord 2-stage RC-filter (out-of-band noise filtered)



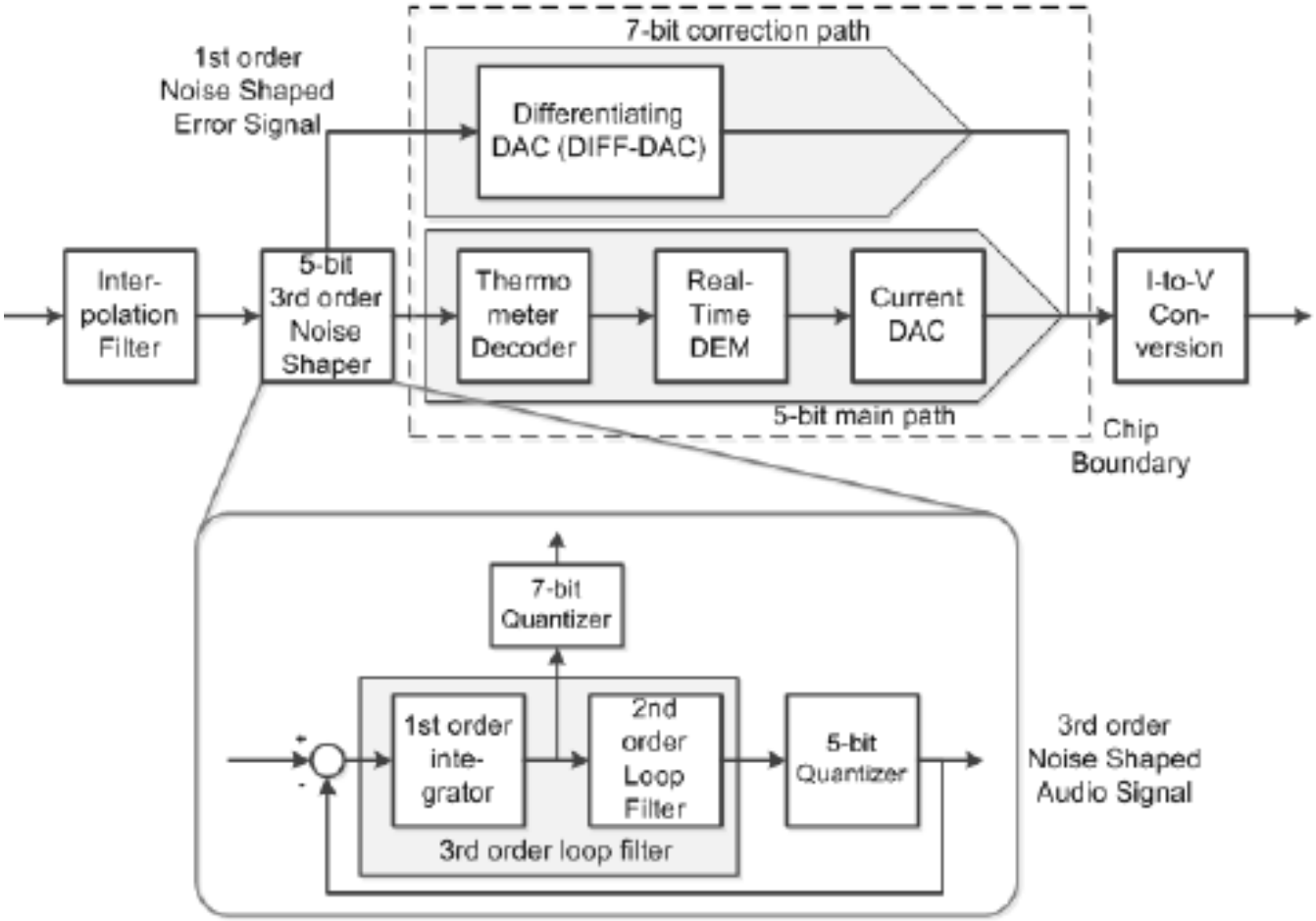
Current Steering ΣΔ-DACs

Approaches to limit the out-of-band noise:
Semi-digital filtering applicable to 1bit SD-modulation



Current Steering ΣΔ-DACs

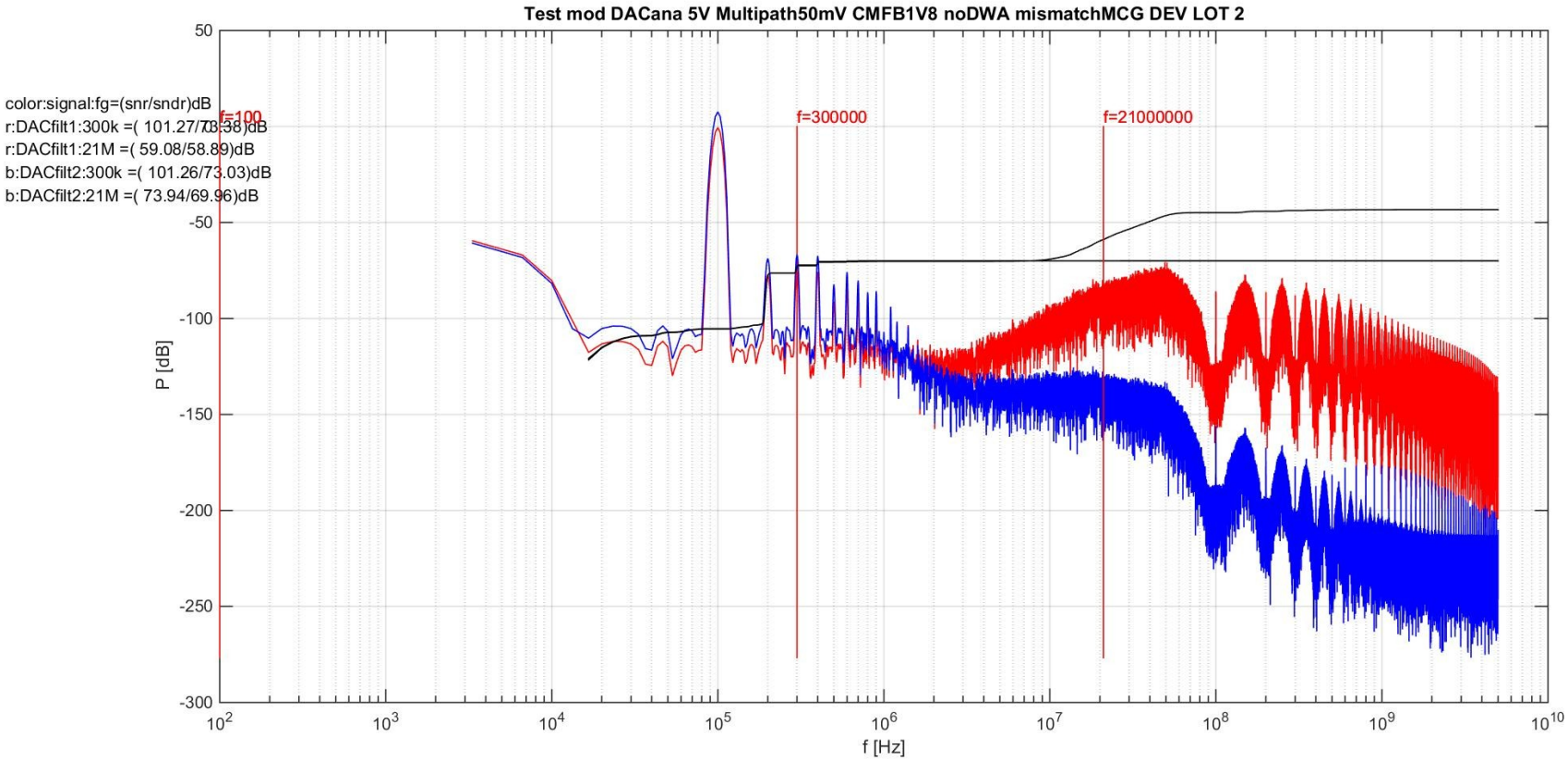
Approaches to limit the out-of-band noise



Current Steering ΣΔ-DACs

Analog output after 3order 2-stage analog Bessel reconstruction filtering: RC-filter with 2 fully differential Amplifiers, no scrambler:

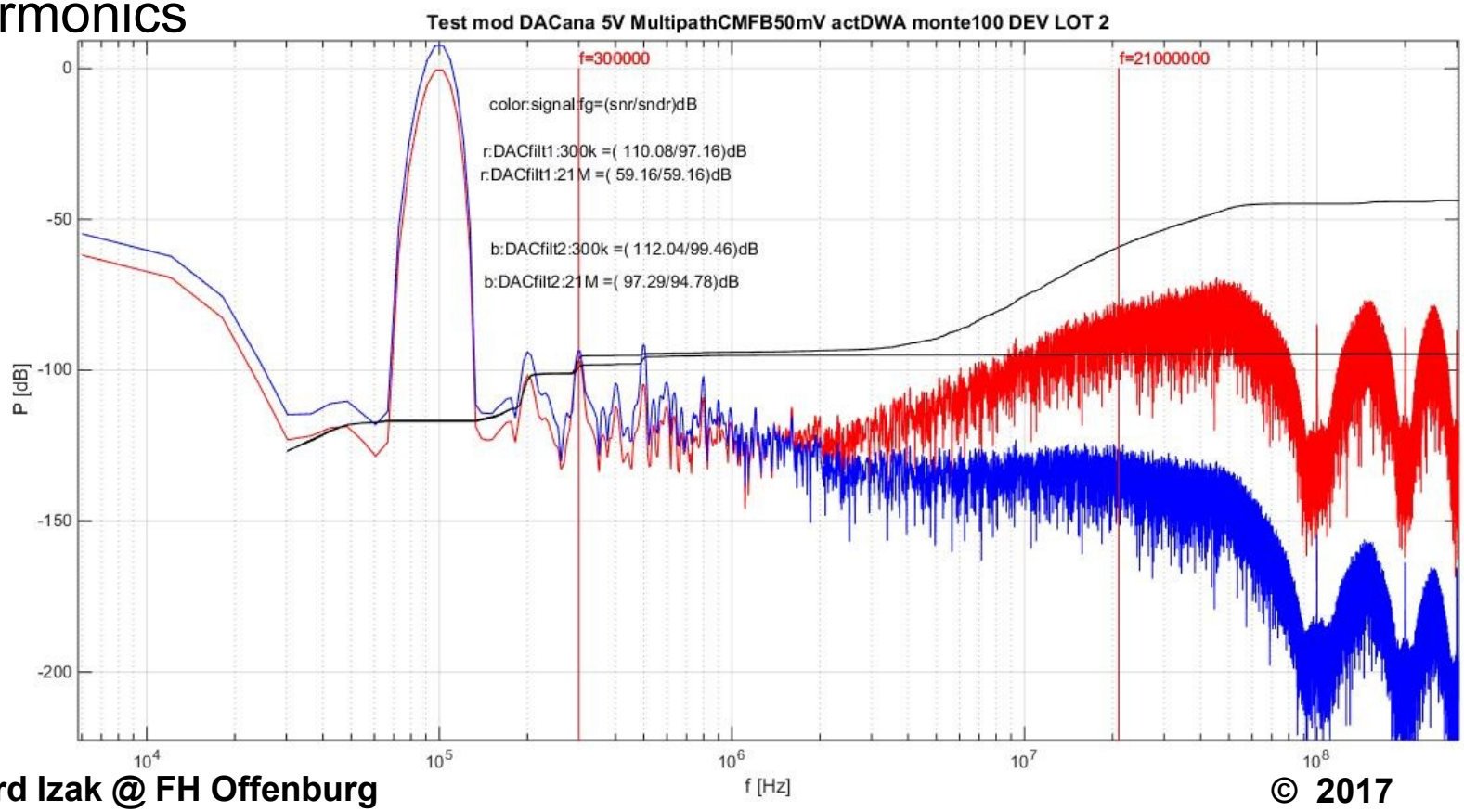
SNR = 101dB in 300kHz, but SNDR = 73dB due to harmonics



Current Steering ΣΔ-DACs

Analog output after 3order 2-stage RC analog Bessel reconstruction filtering: DWA randomizer attenuates the harmonics:

SNR = 110dB in 300kHz, now SNDR = 97dB suppressed harmonics



Summary

- Different DAC topologies discussed
- DAC Specification Parameters reviewed and discussed regarding achievable values
- Oversampling DAC architecture proposed
- Circuit details and design problems
- Simulation setup and verification approaches