Hardware Realisierung eines Pipeline A/D-Wandlers

Hardware Realisation of a Pipeline A/D-Converters

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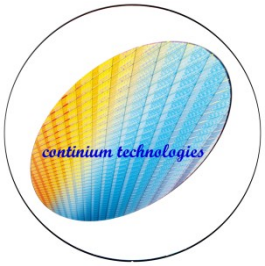


OTH Regensburg, 20.April 2021

Outline

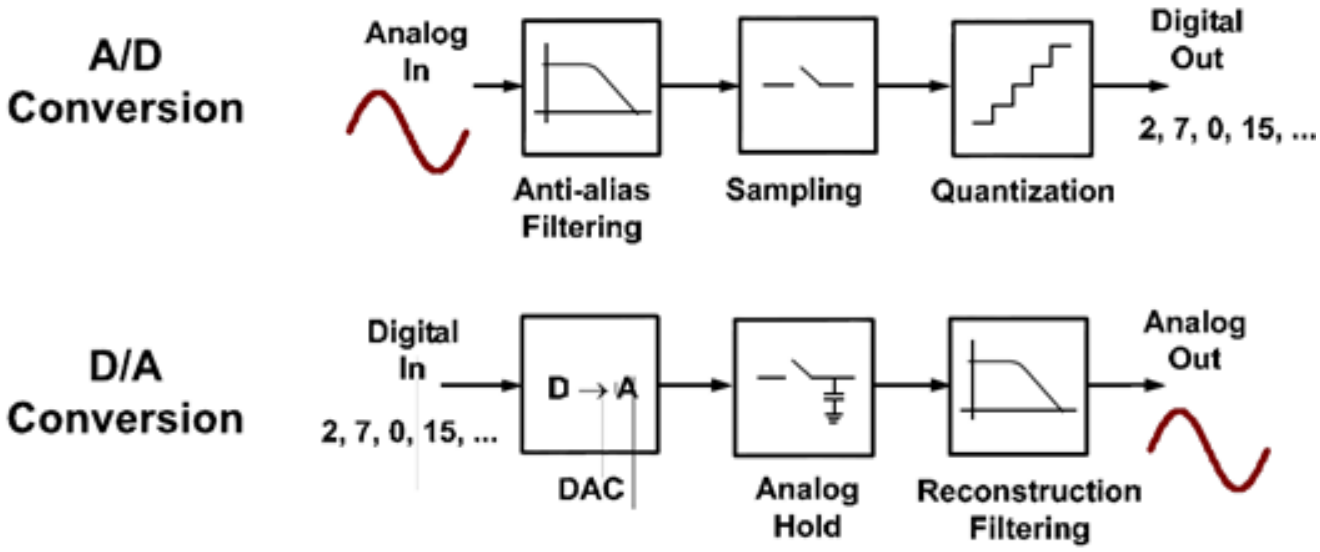
- A/D-Converters: Intro & Architecture differences
- Cyclic ADC => Pipeline ADC: Increasing the sample rate
- Circuitry of a Pipeline-ADCs
- Circuit non-idealities and counter-measures
- Pipeline-ADC modification and new approaches
- Outlook and Summary

Basics of Data Conversion

Each digital signal processing system needs a data acquisition channel, an interface to our analog world: ADC and/or DAC

ADC/DAC circuit design is the most challenging field of electronics:

- each additional bit of accuracy corresponds to a doubled precision requirements: 10bit = 2^{-10} = 0,1% => 20bit = 2^{-20} =1ppm
- design of data converters needs deep understanding of their spectral properties (system theory)



ADC Architectures

ADC contradiction (design compromise): **Speed ⇔ Accuracy**

- high sample rate (GS/s) with low resolution (6-8-10 bit)

  (satCom, early mobCom, digTV)

  parallel ADC: Flash, Folding, (Parallel) Pipeline, Bandpass Σ-Δ/CTSD

- moderate sample (MS/s) rate at moderate resolution (12-14 bit)

  Serial ADC / Weighting principles: successive approx. SAR ADC and cyclic/algorithmic ADC, Σ-Δ ADC, Pipeline ADC

- low sample rate, very high resolution (20-24 bit)

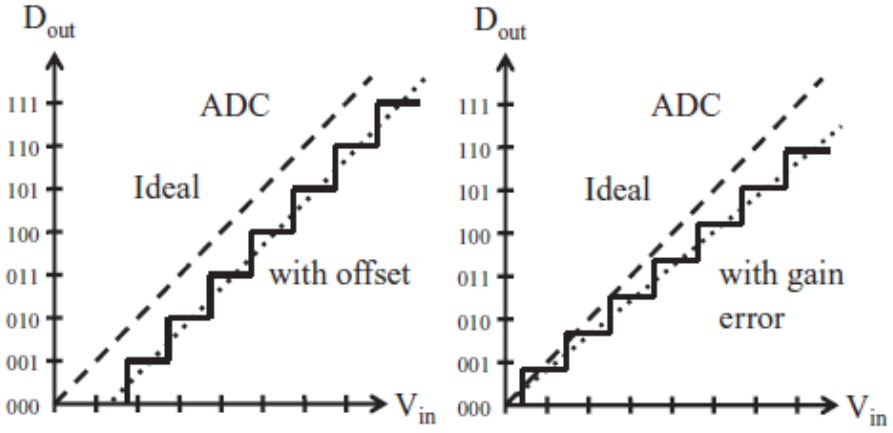
  (process control, precise sensor monitoring, space telescopes)

  - Σ-Δ ADC with high oversampling (OSR)
  - integrating & incremental ADC

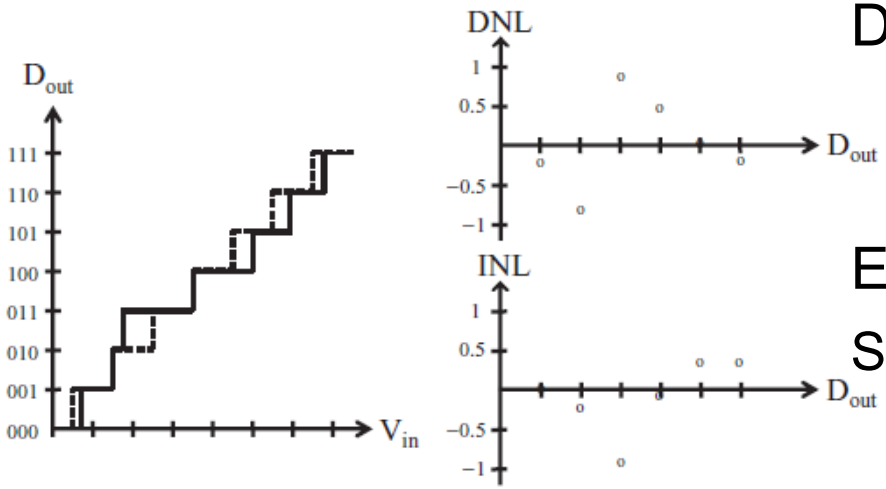
ADC specification parameters

Static parameters

- ADC offset error, ADC gain error (slope)



- Integral (INL) and Differential (DNL) Non-Linearity



Dynamic performance metrics: SNR, SNDR, THD, SFDR in [dB]

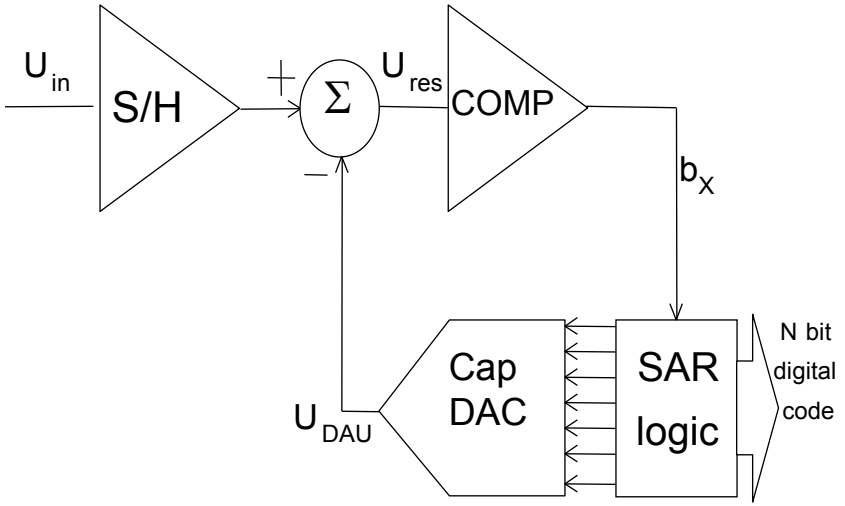
ENOB effect. Number of Bits

SNDR = 6,02.ENOB + 1,76dB

Serial ADC Architectures

Weighting A/D conversion principle: 1-bit conversion cycle

Successive approximation (SAR)

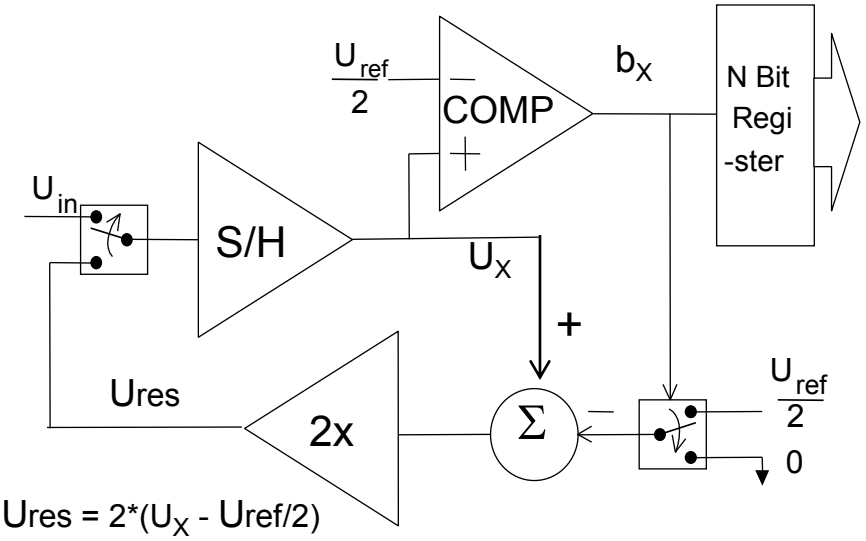


-Simplest circuitry: Comparator, CapArray

=> Higher sampling rate!

- calibration for >11 Bit accuracy required
- large input Cap to be driven (Pre-Amp)
- DAC => key functional block (linearity)

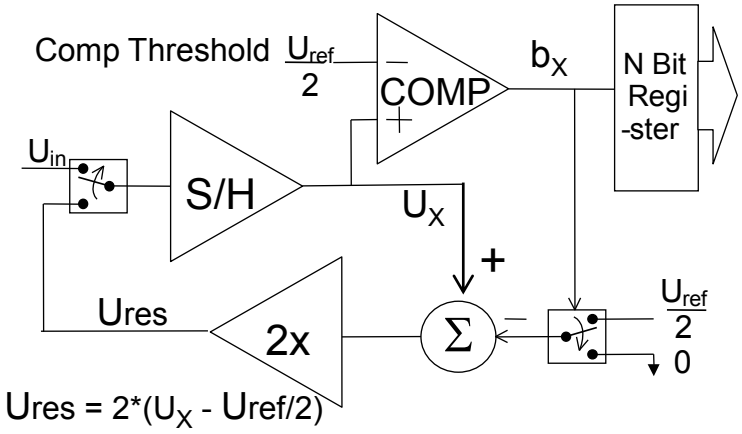
cyclic/algorithmic ADC



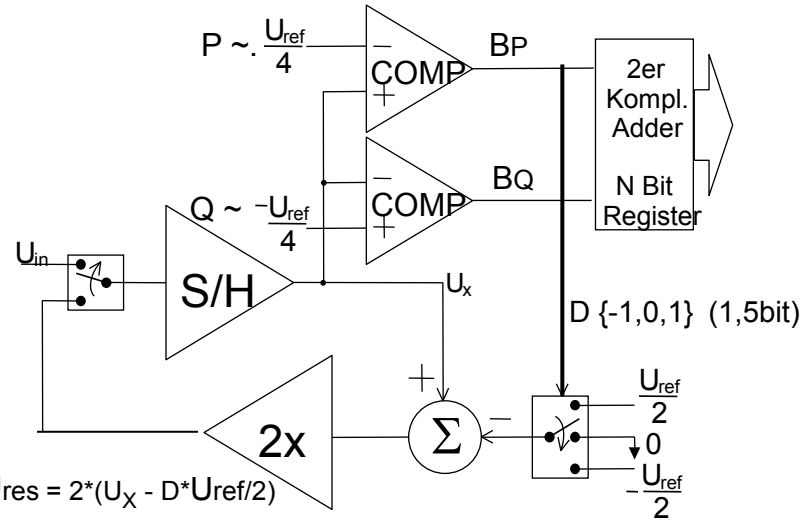
- Full analog circuitry (SC & Amp) =>
  => more R&D complexity
- Offset and Loop-Gain crucial
- Lower area but lower sample rate

Serial ADC: 1b vs. 1.5b cycle

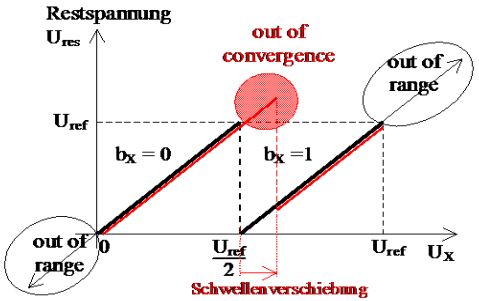
CR: conventional restoring (1b)



RSD: redundant signed digit (1.5b)



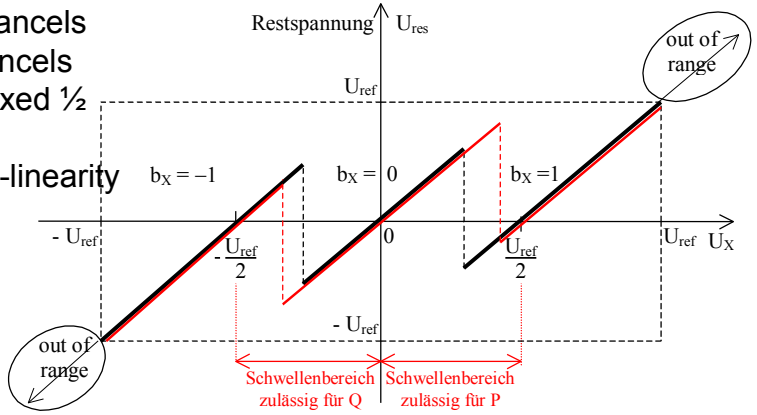
Gray (UC Berkeley) 1984-1990



+ Comp offset cancels
+ Loop offset cancels
+ Loop gain relaxed ½

- Reference non-linearity

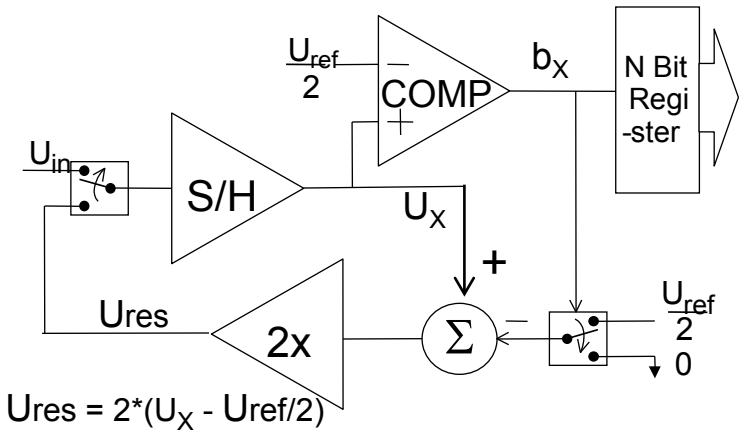
Ginetti SSC'92, Lewis SSC'92



Robertson diagram: depiction of the 1b ADC loop transfer function

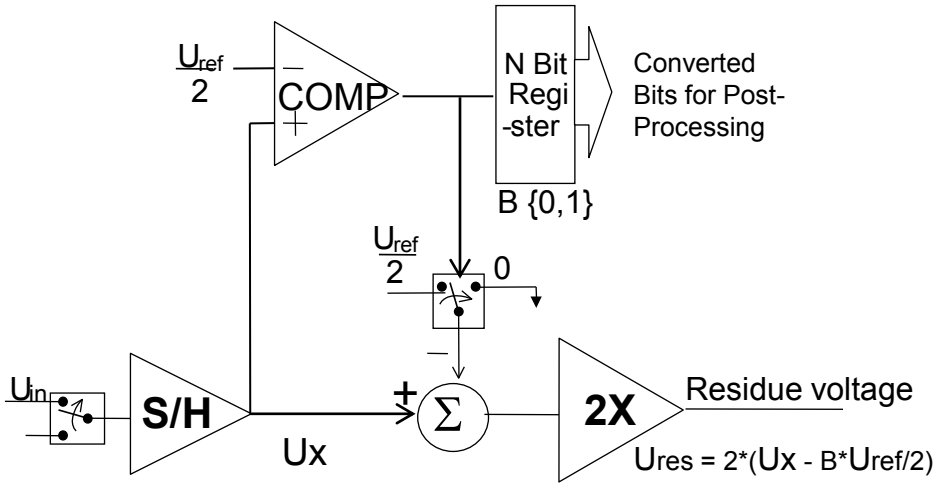
Serial ADC => parallel ADC

Cyclic ADC: 1b conversion loop



Instead of recycling the ADC loop for conversion for all 12-14 bits => break up the loop and pass the converted residue voltage to the next 1b ADC conversion stage

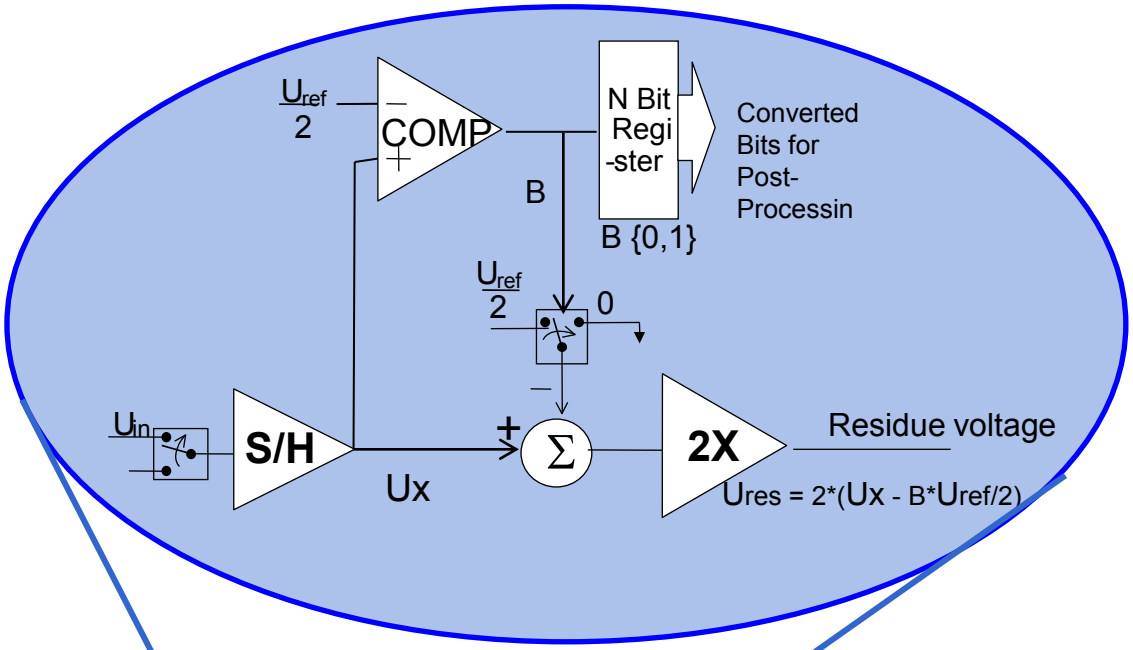
Pipeline ADC: 1b conversion stage



Latency of conversion remains identical, but conversion speed increases! (pipelining principle)

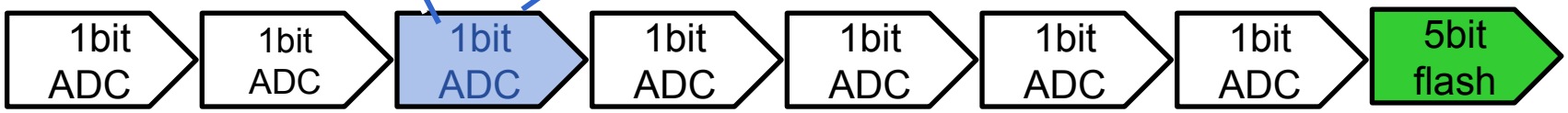
Chip Area and Power Consumption increase (12b pipe => 12x area)

Pipeline ADC

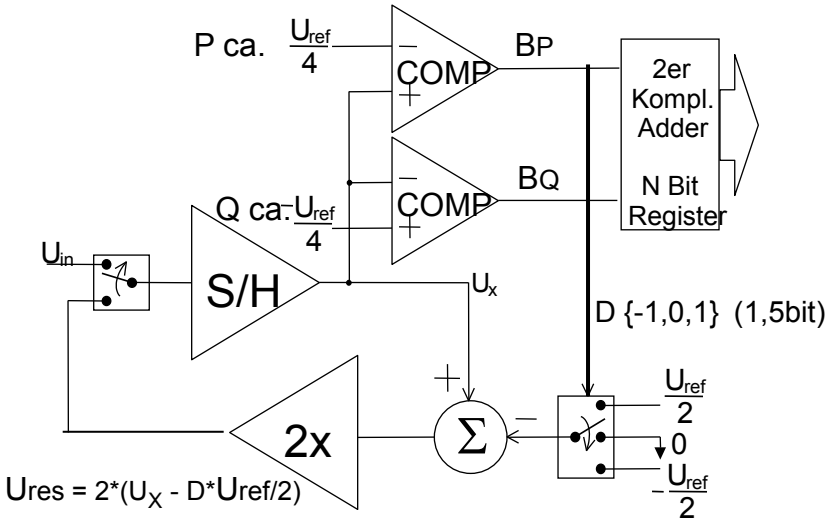


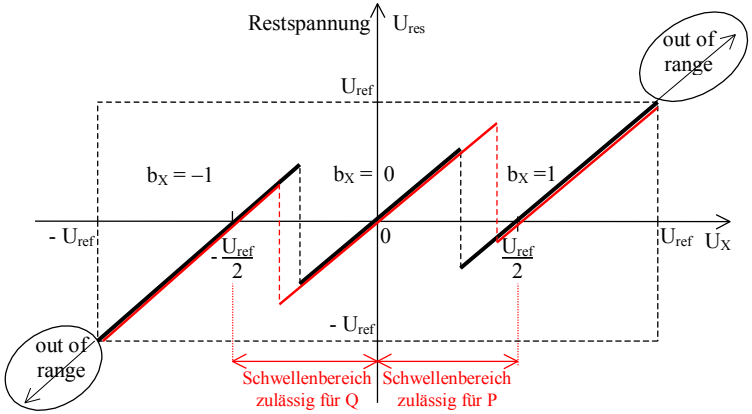
1st stage requires 12b accuracy (SC settling, Amp gain&offset) =>
each following 1b-stages has 1b decreased accuracy requirements
⇒speed (shorter cycles) and power scaling (simpler amplifiers)

⇒ speed increase by including last stage as 5b flash ADC (no residue)



Circuit non-idealities





Switched Capacitor (SC) realization of Sample&Hold (S&H) , Reference subtraction and 2x Multiplication/gain

Analog circuit realization with operational amplifiers (even if simplest voltage doubling technique by stacking capacitor arose in 2000 Quinn @ Xilinx)

Error sources of analog SC circuitry:

co = Comparator offset => Missing Codes and Missing Resolution
1.5b RSD conversion cancels this error

lo = Loop offset => Overall Offset + Non-linaearity
1.5b RSD conversion cancels this error

ro = Reference offset => Overall Gain error

ge = Loop gain (!= 2) error => Error in linearity (INL,DNL)

Circuit non-idealities

- **Dynamic Errors**
  - Sampling- and Jitter-noise (kT/C) => SNR degradation
  - additional effects in the near of the frequency-limit caused by the shortened settling process
    - additional OpAmp-, Sampling-, Jitter- noise
    - Frequency limitation of Amplifier (deterioration of ENOB over fin)

Circuit non-idealities

- **Dynamic Errors**
- **Static Errors (steady state of the settling process)**

affecting in the ADC:

- Offset, Overall gain ➔ calibration after A/D conversion possible
- INL,DNL (=> THD) : mainly caused by loop gain-error (x2-operation)

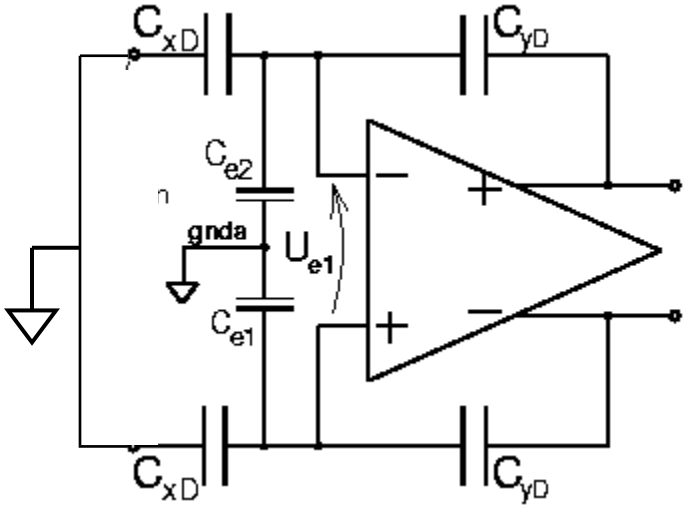
Main physical error-sources and counter-measure solutions :

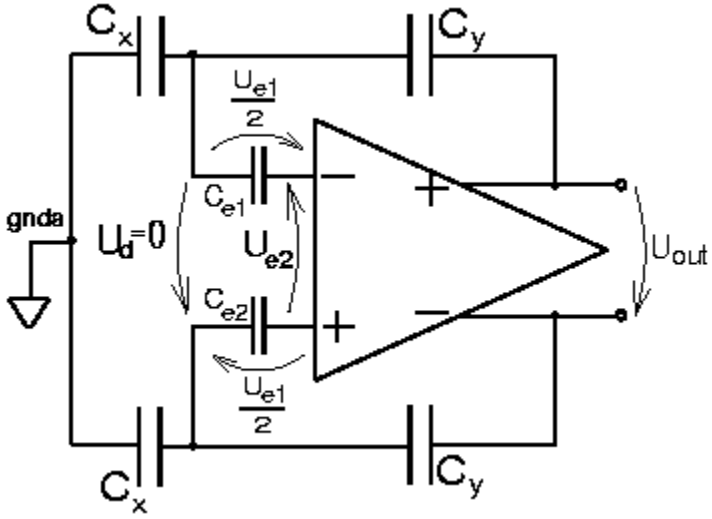
All effects (except offset) deteriorates the accurate x2-operation

- Capacitors : Capacitor-Mismatch ➔ Ratio independent SC design
- Switches : Clock-Feedthrough ➔ Fully-Differential Technique
  Charge-Injection ➔ Bottom-Plate-Sampling
- OpAmp: Offset & Finite Gain ➔ CDS Techniques | High Gain
- Parasitic Caps: ➔ stray insensitive design, post-layout analysis → layout

SC error compensation

CDS: correlated double sampling (additional SC phase with dummy Caps) => voltage correction





Prediction phase (error measure):

Transfer operation with Dummy-C's for error estimation

$C_{e1}=C_{e2}$

➔ $U_{Ce1} = U_{Ce2} = ½Ue1$

$C_{xd} / C_{yd} = C_x/C_y$

➔ Uoutd ≈ Uout

➔ Ue1 ≈ Ue2

but because of charge needed by Ce:

$Ue2 = (1+\varepsilon)* Ue1; \quad \varepsilon \approx (1/G_0)*(C_e/C_y)$

Operation phase (error compensation):

final Transfer operation with error cancellation

Ue2 - (2 * ½ Ue1) ≈ 0

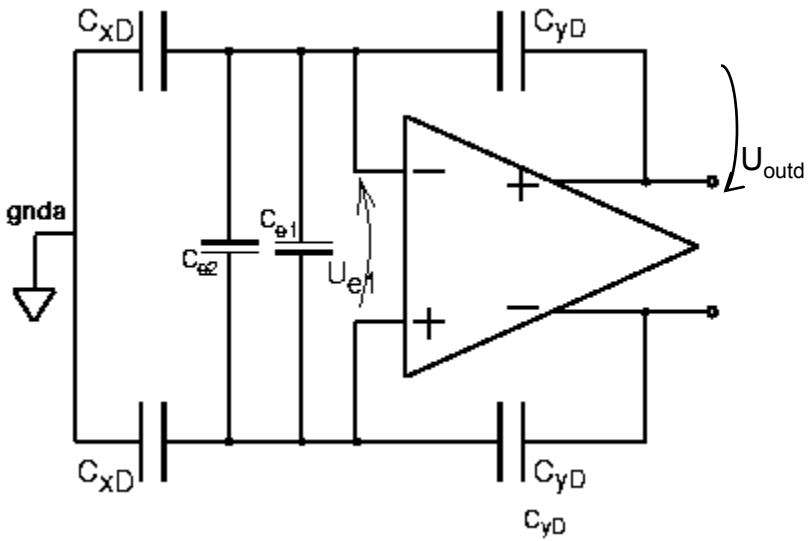
➔ **new virtual ground nodes with zero-difference**

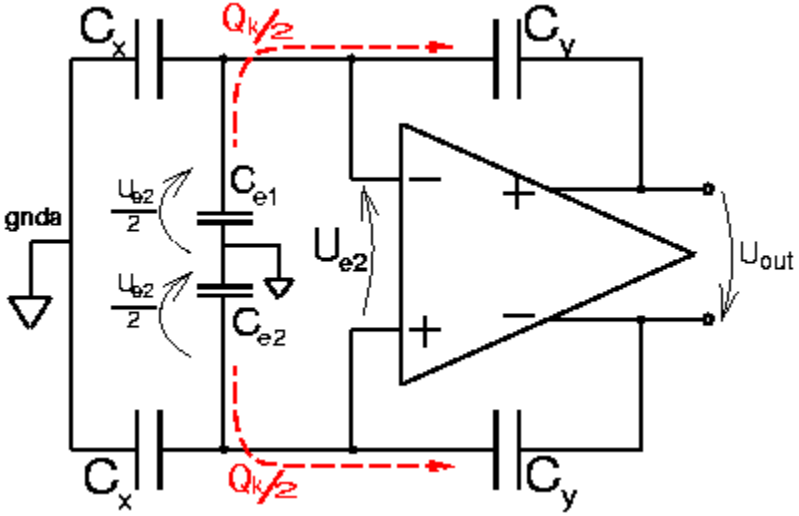
➔ **full charge transfer from C_x to C_y**

Exact Size of Ce doesn't matter , because of voltage addition

SC error compensation

CDS: correlated double sampling => charge correction





Prediction phase:

Transfer operation with Dummy-C's for error estimation

$C_e = C_{e1} = C_{e2} = C_x + C_y \approx 2 * C_x$ with $C_x \approx C_y$

➔ $Q_{Ce} = Ue1 * (C_{e1} + C_{e2}) \approx 4 * Cx * Ue1$

$C_{xd} / C_{yd} = C_x / C_y$

➔ Uoutd ≈ Uout ➔ Ue1 ≈ Ue2

but because of charge needed by Ce:

$Ue2 = (1+\varepsilon) * Ue1; \quad \varepsilon \approx 2/G_0$

Operation phase :

final Transfer operation with error compensation

Charge in Ce will be reduced by Qk

$Qk = 2 * C_e * (Ue1 - ½ * Ue2) \approx C_e * Ue2$

Error at output is (see before !):

$Ue_{out} = Ue2 * (1 + C_x/C_y) \approx 2 * Ue2$

➔ **needed compensation charge is $Ue_{out} * Cy$**

➔ $Qk' = Ue2 * (C_x + C_y) \approx 2 * C_y * Ue2$

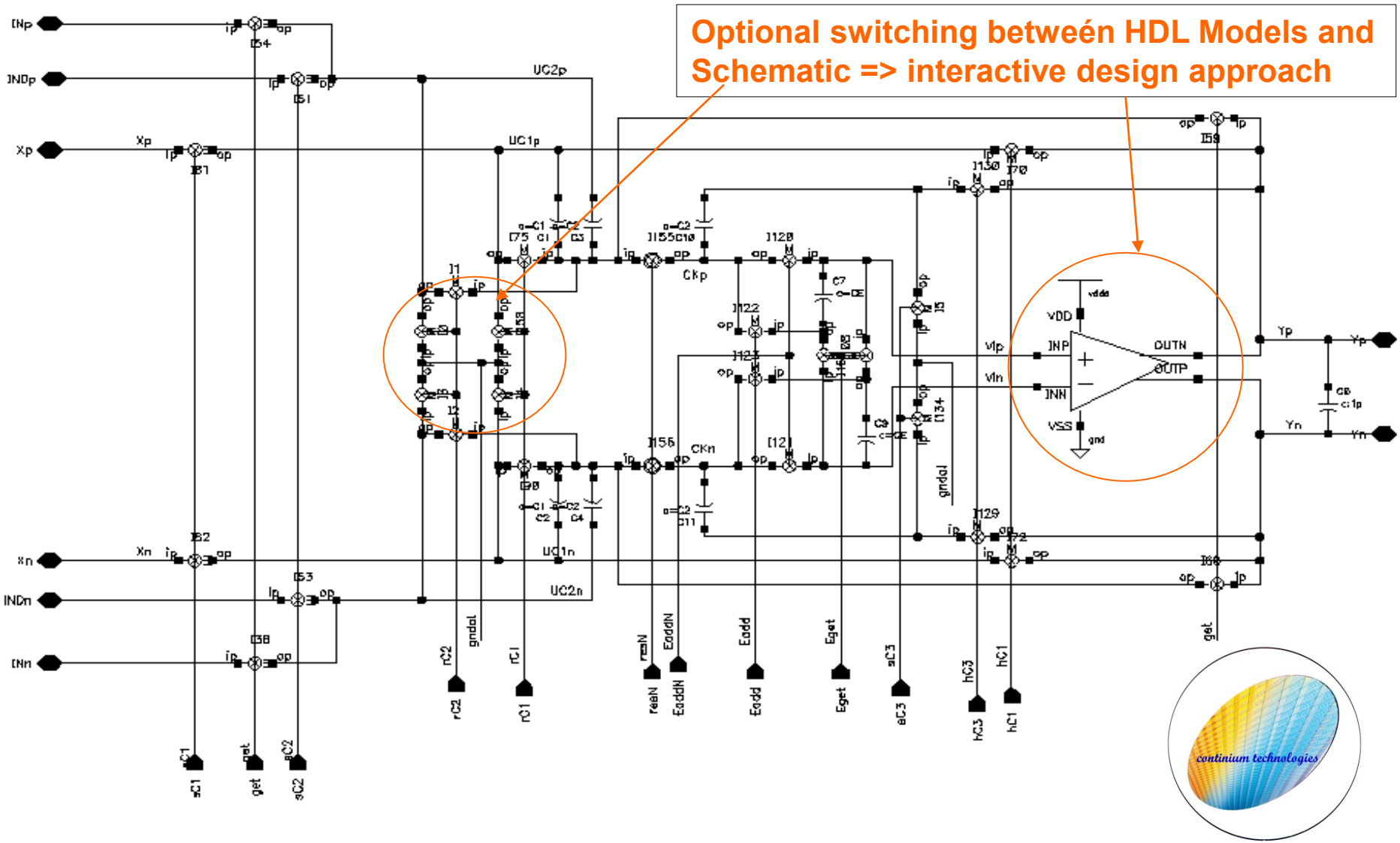
➔ **Correction is done if Qk'=Qk:** $C_e = C_x + C_y \approx 2 * C_y$

considering charge consumption of Ce (if Cx = Cy):

exactly: $C_e = 2 * C_x * (1 + \varepsilon) / (1 - \varepsilon)$

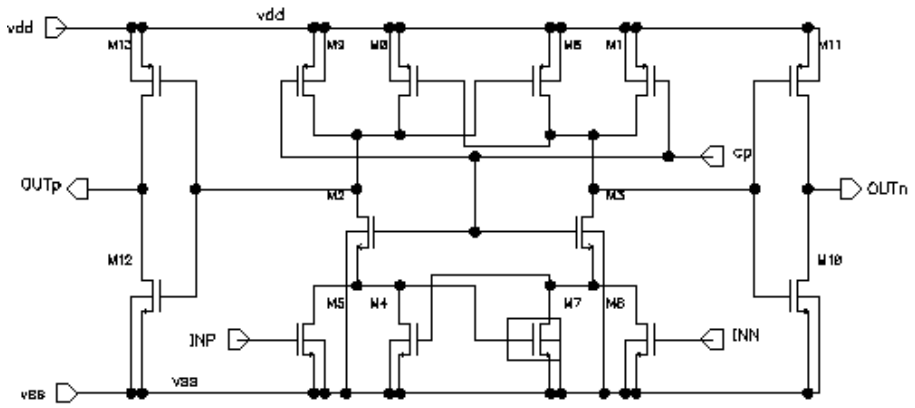
Kindt, Izak: ADDA 2002 Prague publication

SC error compensation



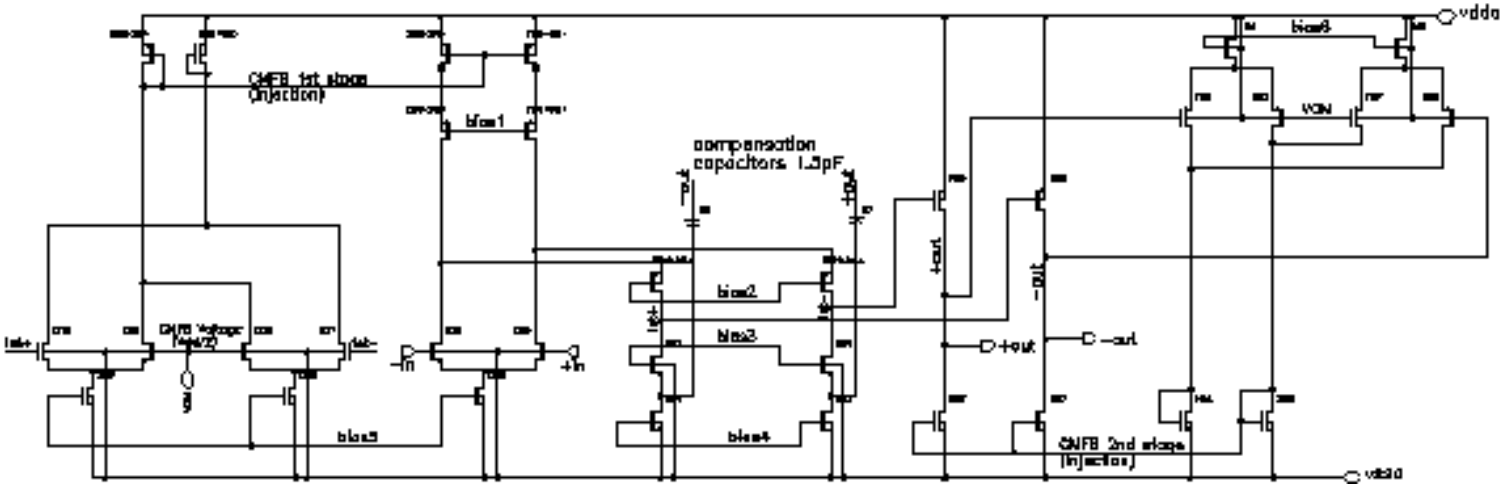
Block level circuit design

Clocked comparator (SC)



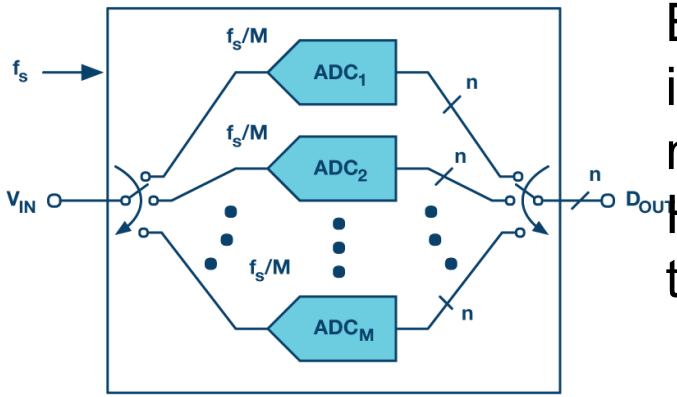
Amp spec	ADC1 (2 stages)	ADC2 (1 stage)
Diff. Gain	101.3 dB	85.5 dB
Unity gain freq. (@ 2pF load)	68.5 MHz	34 MHz
Phase margin (@ 2pF load)	55.7º	71º
Power consumpt.	28 mW	4.3 mW
Chip area	1.5 mm^2	0.11mm^2
Internal compensat.	1.5pF	--

0.6um CMOS in 1999



Recent innovation in pipeline ADC

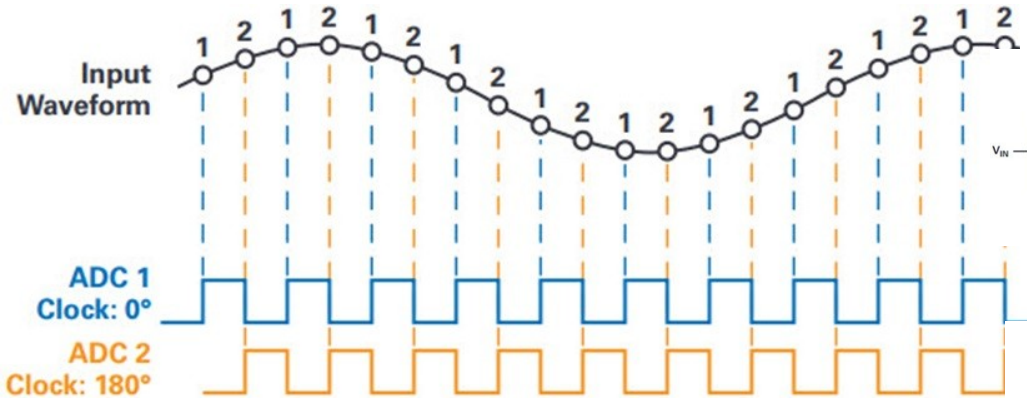
Time-interleaving (parallel pipeline)

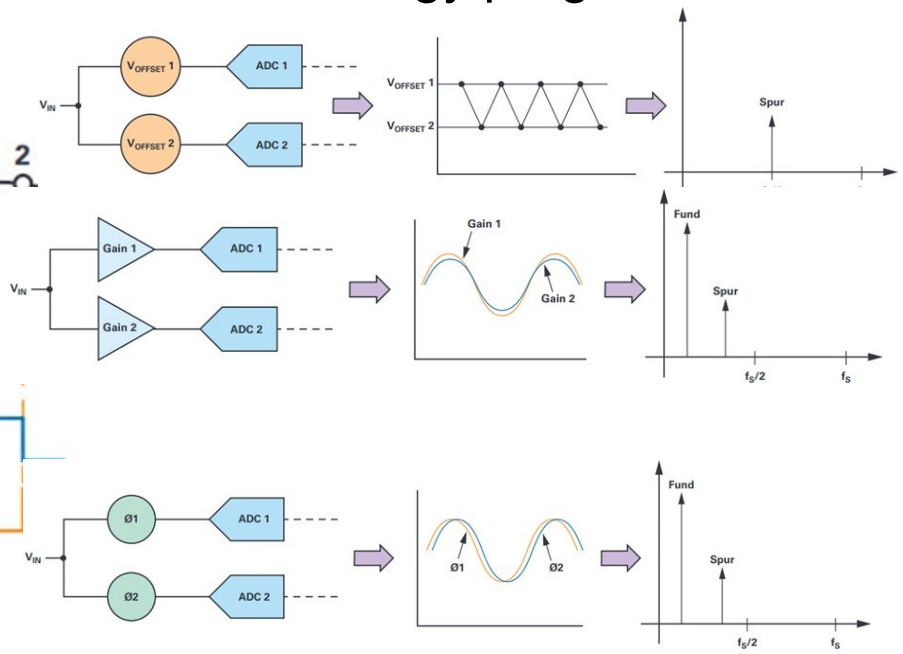


Highest speed boost of ADC in recent years: Ahmed Ali (ADI) 14b 5GS/s in 28nm CMOS

But new challenges arose: digital calibration of inter-channel offset, gain, clock skew, BW mismatch!

Huge digital post-processing, possible only thanks to 12-20nm technology progress!

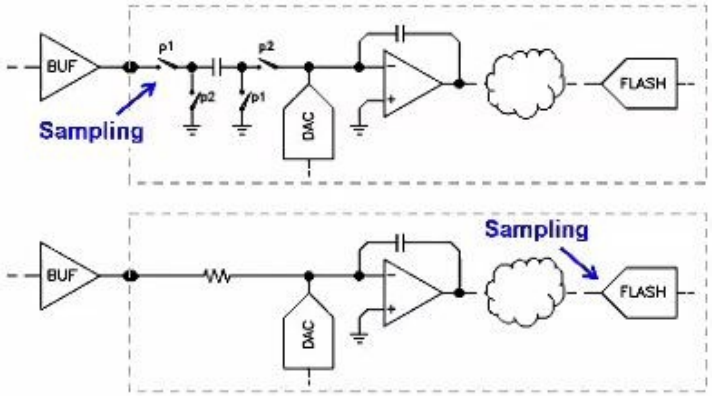




Recent innovation in pipeline ADC

Continuous-Time pipeline ADC

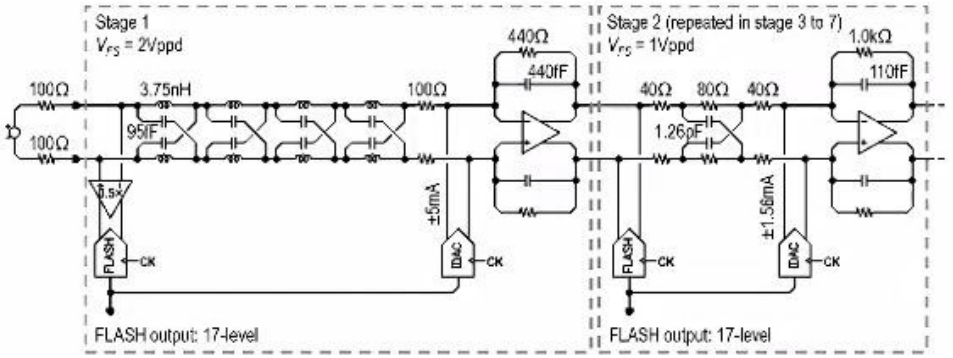
Inherent Anti-Aliasing: DT & CT ADC



CT offers inherent anti-aliasing
→ Anti-aliasing filter can be relaxed or removed

Combining the advantages from both worlds:
-SC pipeline ADC with large bandwidth
- inherent AAFilter & silent input of CTSD ADC

5-Stage CT Pipelined ADC in 28nm CMOS [2]



Gubbins/Moon: 2008-2010 publication

Shibata (ADI) 2019-2020 publications

Summary

- Pipeline ADC architecture derived
- Non-idealities at system and circuit level discussed
- Circuit blocks and design solution revealed
- Further innovation for future pipeline ADCs shown